Low-Temperature Growth for 3D Integration of 2D Materials

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The integration of novel logic and memory devices, fabricated from van der Waals materials, into CMOS process flows with a goal of improving system-level Energy-Delay-Product (EDP) for data abundant applications will be discussed. Focusing on materials growth and integration techniques that utilize non-equilibrium, kinetically restricted strategies, coupled with in-situ characterization, enables the realization of atomic configurations and materials that are challenging to make but once attained, display enhanced and unique properties. These strategies become necessary for most future technologies where thermal budgets are constrained and conformal growth over selective areas and 3-dimensional structures are required.

In this work, we demonstrate the high-quality MBE heterostructure growth of various layered 2D materials by van der Waals epitaxy (VDWE). The coupling of different types of van der Waals materials including transition metal dichalcogenide thin films (e.g., WSe_2, WTe_2, $HfSe_2$), helical Te thin films, and topological insulators (e.g., Bi_2Se_3) allows for the fabrication of novel electronic devices that take advantage of unique quantum confinement and spin-based characteristics. We demonstrate how the van der Waals interactions allow for heteroepitaxy of significantly lattice-mismatched materials without strain or misfit dislocations. Yet, at the same time, the VDW interactions are strong enough to cause rotational alignment between the epi-layer and the substrate, which plays a key role in the formation of grain boundaries. We will discuss TMDs, Te, and TIs grown on atomic layer deposited (ALD) high-k oxides on a Si platform as well as flexible substrates and demonstrate field-effect transistors with back-end-of-line compatible fabrication temperatures (<450 °C). High performance transistors with field-effect mobilities as high as 400 $cm^2/V\text{-}s$ are demonstrated. The achievement of high-mobility transistor channels at BEOL compatible processing temperatures shows the potential for integrating van der Waals materials into CMOS process flows.

This work was supported in part by the Center for Low Energy Systems Technology (LEAST), one of six centers supported by the STARnet phase of the Focus Center Research Program (FCRP), a Semiconductor Research Corporation program sponsored by MARCO and DARPA. It is also supported by the New LIMITS Center and the SWAN center, SRC centers sponsored by the Nanoelectronics Research Initiative and NIST.

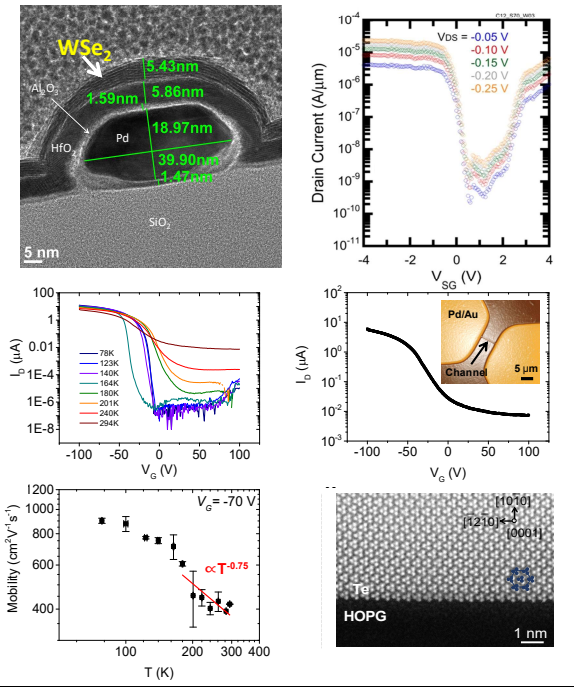

Figure 1: TEM and device characteristics of WSe_2 and Te thin films grown by MBE at low-temperature.