Graphene/Insulator/Silicon MOS Capacitors: Fowler-Nordheim Tunneling and Quantum Capacitance

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Abstract

Although mostly studied as a channel material in transistors, graphene is also a promising candidate as the gate electrode in metal-oxide-semiconductor (MOS) devices, particularly when transparency, mechanical flexibility, or workfunction tunability is a requirement [1-3]. Here, we fabricate and study MOS capacitors with graphene as the gate electrode and silicon as the semiconductor. We find that Fowler-Nordheim (F-N) tunneling dominates the gate tunneling current in these devices for oxide thicknesses of 10 nm and larger, whereas for devices with 5 nm oxide, direct tunneling also starts to play a role. Furthermore, we study the temperature dependence of the F-N tunneling current in these devices in the temperature range 77 to 300 K. We extract the pre-exponential and exponential F-N coefficients and the effective tunneling barrier height as a function of temperature. In addition, we experimentally and theoretically study the effect of the quantum capacitance of graphene on the total gate capacitance of graphene/insulator/silicon MOS structures. Using the modified density of states of graphene in the presence of charged impurities, we numerically compute the quantum capacitance of graphene as a function of the graphene electrostatic potential at different temperatures and strengths of the potential energy fluctuations. We compare the exact results to various analytical approximations made in the literature when fitting experimental data. Furthermore, we numerically simulate the full *C-V* characteristics of these devices at different values of the equivalent oxide thickness, silicon doping density, and graphene Dirac voltage. Finally, we fit our experimental *C-V* data obtained at different oxide thicknesses in order to extract the strength of the potential energy fluctuations and the parasitic impedances. Our results provide important insights into the potential use of graphene as a gate electrode in MOS technology.

References

[1] Y. An, A. Behnam, E. Pop, G. Bosman, and A. Ural, J. Appl. Phys. **118** (2015) 114307.

[2] Y. An, A. Shekhawat, A. Behnam, E. Pop, and A. Ural, Appl. Phys. Lett. **109** (2016) 223104.

[3] Y. An, A. Shekhawat, A. Behnam, E. Pop, and A. Ural, MRS Advances **2** (2017) 103.

Figures

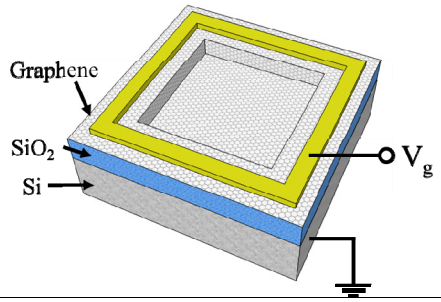

Figure 1: Schematic of the fabricated device

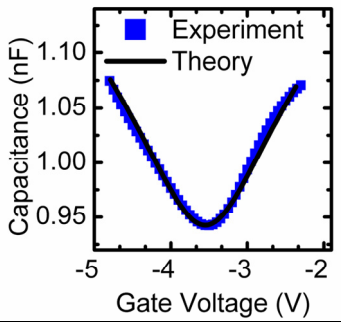

Figure 2: The local minimum in the *C-V* data measured for a thin oxide capacitor under accumulation and the theoretical best-fit taking into account the quantum capacitance of graphene in the presence of charged impurities