Epitaxial graphene (EG) on silicon carbide (SiC) is promising for fabrication of graphene field-effect transistors (GFETs) because it can be formed directly on a large-size, semi-insulating substrate without any transfer procedures. For fabrication of high performance GFETs minimizing the step edges underneath the grown EG is essential because they can lead to increase of the channel resistance [1]. To this goal, we here propose a new method, a modified hydrogen annealing process. The method consists of (1) a low-temperature (LT) annealing in H2 at 500 °C for 5 hours for the SiC surface reconstruction and (2) a subsequent high-temperature (HT) annealing in Ar/H2 at 1480 °C for the graphene growth. Figure 1(a) shows the surface morphology of a 6H-SiC(0001) wafer after the LT-H2 annealing. A well-ordered surface, with a step height of 1.1 nm and a terrace width of 1.5 μm, was formed. Using this substrate, graphene was grown in either Ar (1420 °C) or in Ar/H2 ambient (1480 °C). The EG grown in Ar ambient (Fig. 1(b)) showed a minimum-step-bunching with a step height of 1.5 nm and a terrace width of 5.0 μm. The EG grown in Ar/H2 ambient (Fig. 1(c)) showed a maximum step-bunching with high steps (~45 nm) and wide terraces (~30 μm). More importantly, the EG grown under the Ar/H2 ambient exhibited a sharper and a higher Raman G'-peak in the spectrum, which indicates formation of a high quality graphene. Figure 2 compares the electrical characteristics of the two EGs. As shown in Fig. 2(a), the EG grown in Ar/H2 ambient exhibits a higher Hall mobility (2095 cm2/Vs) than that grown in Ar ambient (1750 cm2/Vs). The transconductance of the GFETs is also higher in the former (8.87 mS/mm, Fig. 2(c)) than in the latter (0.42 mS/mm, Fig. 2(b)). This improvement is ascribed to the H2-termination of the Si dangling bonds underneath the buffer layer without breakage of the Si-C covalent bond between SiC and the buffer layer [2]. This was confirmed by the appearance of Si-H bond component in the X-ray photoelectron spectroscopy (XPS) analysis. Moreover, a wide terrace width of EG grown in Ar/H2 ambient is advantageous for minimizing the step edges in the GFET channel region, which leads to reduction of the channel resistance. This is the first report to form EG by annealing SiC in Ar/H2, which provides a novel, excellent method to fabricate high quality EG to be used in graphene based electronic devices.

References


Figures

Figure 1: (a) AFM image of LT H2-annealed SiC surface. AFM and Raman spectrum of EG surface grown in (b) Ar and (c) Ar/H2 ambient.

Figure 2: (a) Comparison of Hall mobility of EG grown in Ar and Ar/H2 ambient. Electrical characteristics of GFETs with grown in (b) Ar and (c) Ar/H2 ambient.

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