Direct Graphene Growth and Characterization : in the aspects of Interconnect Application

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In the rapid progress towards miniaturization of nano-scale devices, there are fundamental issues in the development of the next generation interconnect between the devices. According to ITRS (International Technology Roadmap for Semiconductors), the line widths of interconnects are gradually decreased by 2nm per year and their resistivity is exponentially increased. Until now, reduction of resistance has been realized mainly through the optimization of metallization by substrate bias injection. However, these technologies are insufficient to compensate for the resistance increase according to the thickness reduction. Instead, revolutionary new materials and process are required to address long-term scaling down of interconnects.

Graphene has been suggested as a promising material because of its unique electrical and chemical properties. Graphene have been shown to have high current density and its hexagonal lattice is adaptable to prevent chemical diffusion. In addition, high thermal conductivity and extremely strong mechanical strength make them attractive and suitable for nanoscale interconnects. Although high-quality graphene can be produced on catalyst metals, their practical applications, especially Si technologies, are limited by the high-temperature growth and the post-transfer process.

So, in this presentation, we propose a method to grow nanocrystalline graphene (nc-G) directly on silicon wafer, up to 300mm in diameter. We also evaluate the various nc-G characteristics and linked it to a role in the interconnect system. Our work shows the possibility of direct nc-G growth and its application in the present Si integration process.