Multiple Physical Time Scales and Dead Time Rule in Few-Nanometers Sized Graphene-SiO_x-Graphene Memristors

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The resistive switching behavior in SiO_x-based phase change memory devices confined by few nanometer wide graphene nanogaps [1] is investigated. Our experiments and analysis reveal that the switching dynamics is not only determined by the commonly observed bias voltage dependent set and reset times. We demonstrate that an internal time scale, the dead time, plays a fundamental role in the system's response to various driving signals. We associate the switching behavior with the formation of microscopically distinct SiO_x amorphous and crystalline phases between the graphene electrodes. The reset transition is attributed to an amorphization process due to a voltage driven self-heating; it can be triggered at any time by appropriate voltage levels. In contrast, the formation of the crystalline ON state is conditional and only occurs after the completion of a thermally assisted structural rearrangement of the as-quenched OFF state which takes place within the dead time after a reset operation. Our results demonstrate the technological relevance of the dead time rule which enables a zero bias access of both the low and high resistance states of a phase change memory device by unipolar voltage pulses [2].

References

[1] M. El Abbassi, L. Posa, P. Makk, C. Nef, K. Thodkar, A. Halbritter and M. Calame, Nanoscale, 9 (2017) 17312.
[2] L. Posa, M. El Abbassi, P. Makk, B. Santa, C. Nef, M. Csontos, M. Calame and A. Halbritter, Nano Letters, 17 (2017) 6783.

Figures

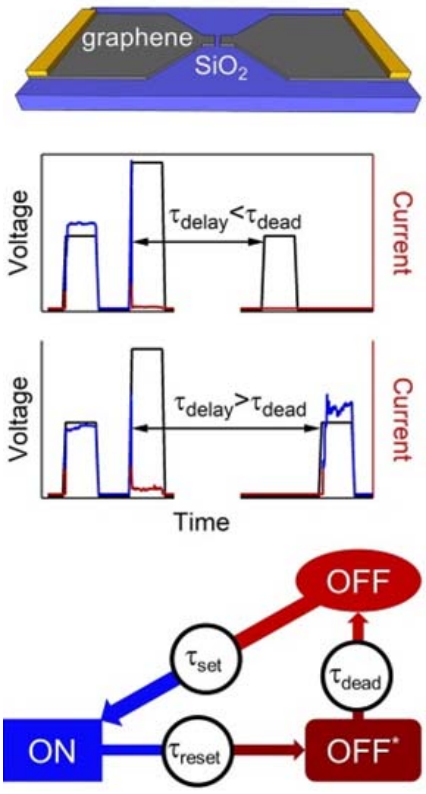

Figure 1: Typical device layout with a 1-3 nm wide nanogap created across a 400 nm wide graphene nanostripe. After initialization in the OFF state and a subsequent zero bias waiting period, a set voltage pulse is applied. However, the corresponding set transition is only achieved when the waiting time exceeds a certain threshold (dead time).