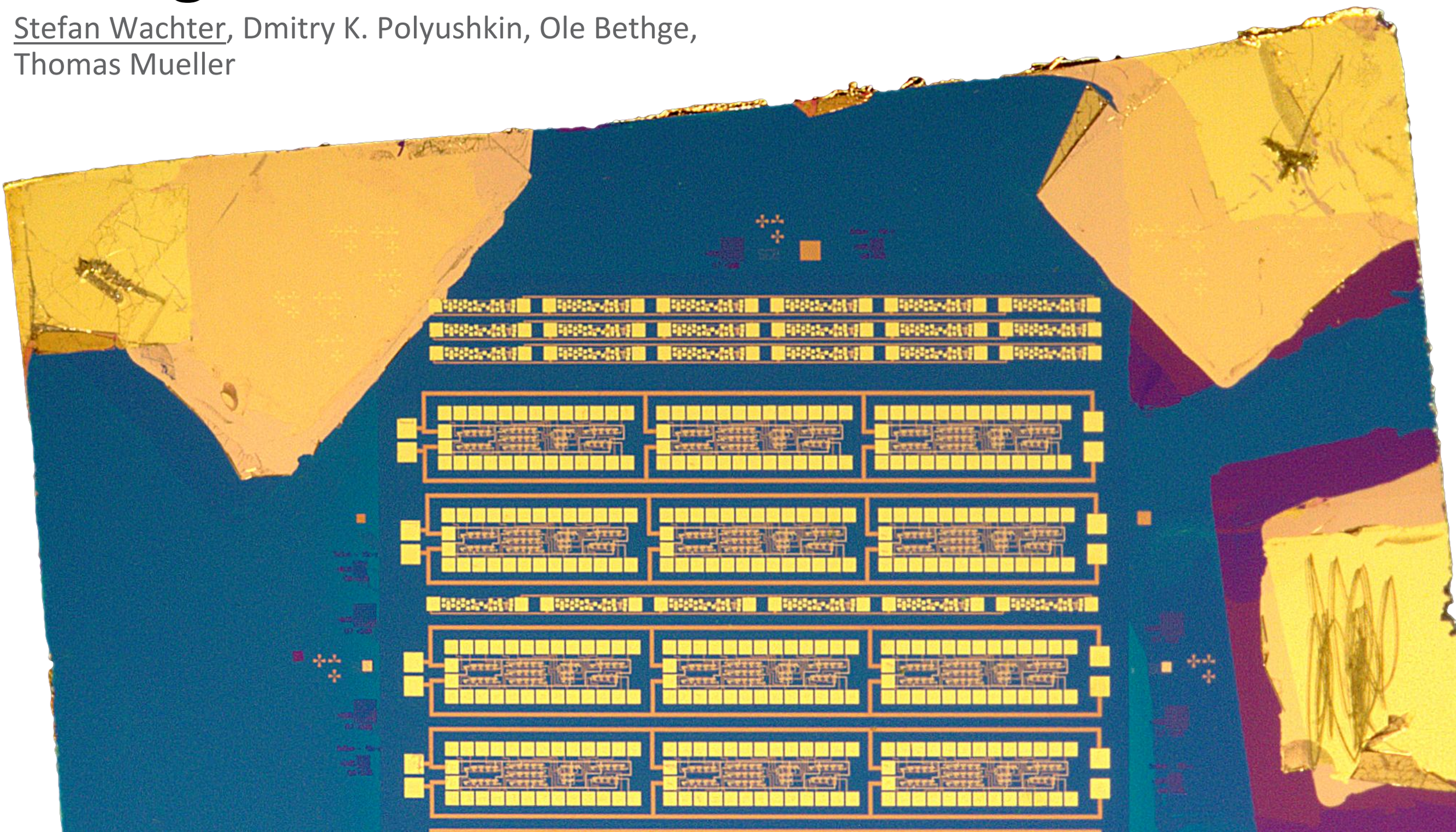
TECHNISCHE UNIVERSITÄT WIEN
Vienna University of Technology

Der Wissenschaftsfonds.

GRAPHENE FLAGSHIP

2D digital electronics

Stefan Wachter, Dmitry K. Polyushkin, Ole Bethge, Thomas Mueller



2D Electronics?

2D materials offer:

- improved electrostatic control
- low sub-threshold slope (TFET)
- no short channel effects

which ultimately results in:

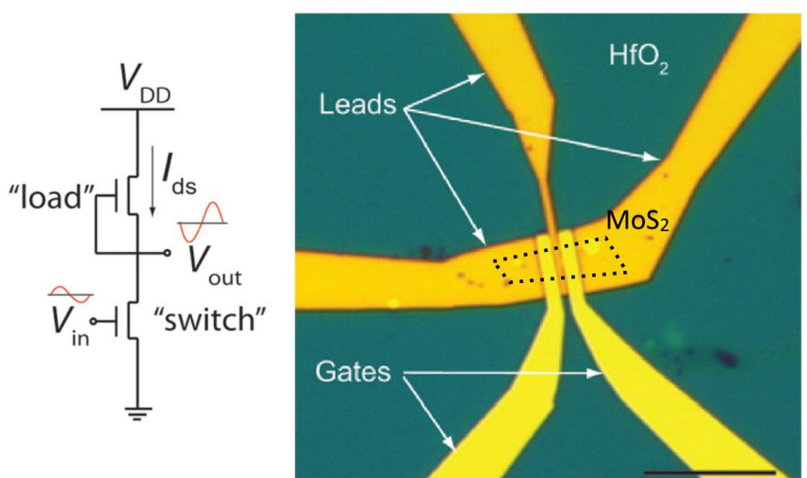
- larger integration density
- low power consumption

in addition:

- flexible
- transparent

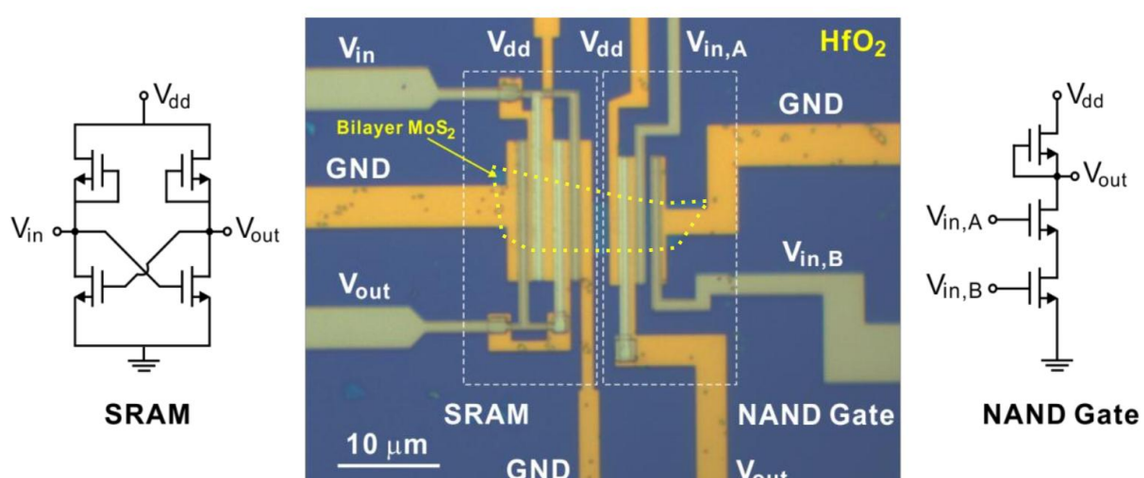
Complexity of 2D semiconductor circuits

- analog circuits



Kis-group (EPFL)

- digital circuits

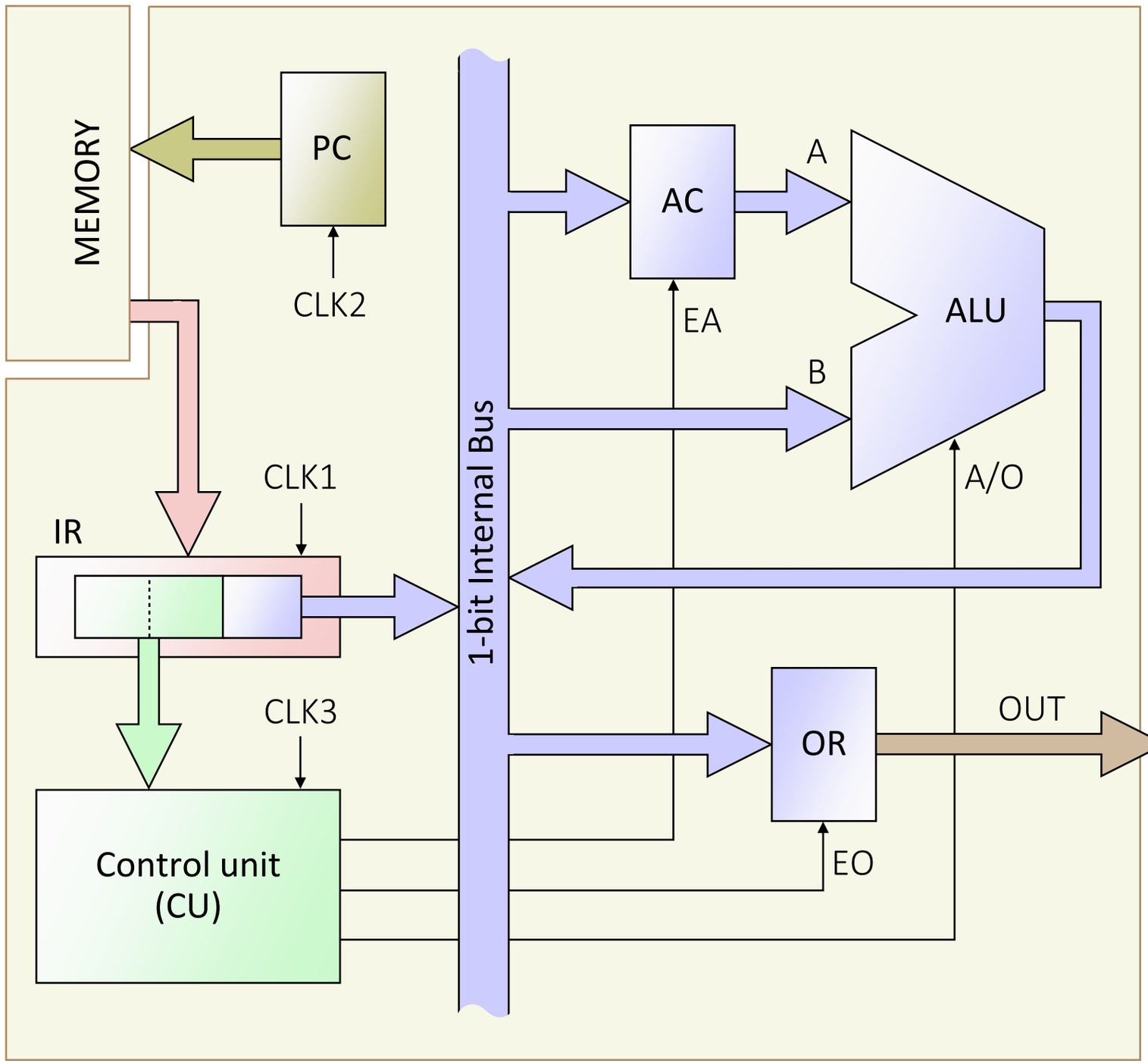


Palacios-group (MIT)

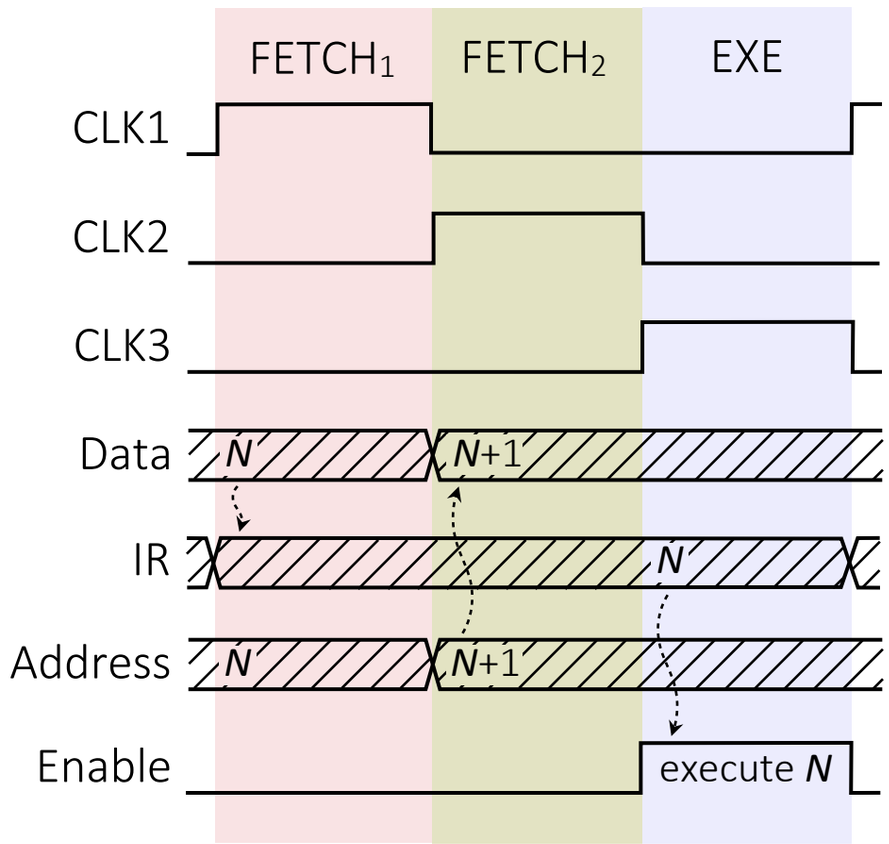
		Complexity	2D semiconductor-based circuits
SSI	Small-scale integration	1-10	State-of-the-art
MSI	Medium-scale integration	10-100	
LSI	Large-scale integration	100-100.000	
VLSI	Very large-scale integration	>100.000	

*Computer Networks (A.S. Tanenbaum)

MoS_2 microprocessor architecture



Timing diagram:



Instruction set:

Command	Code	Example
NOP	00	NOP
LDA	01	LDA 0
AND	10	AND 1
OR	11	OR 0

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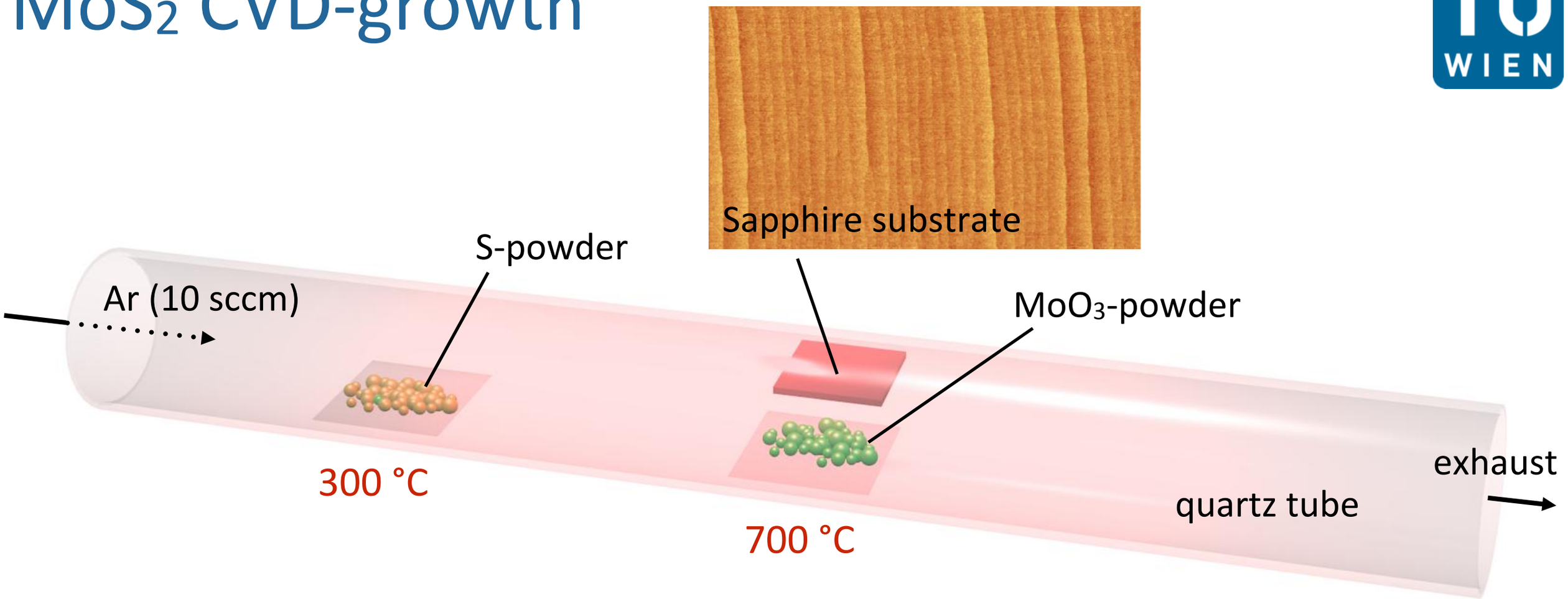
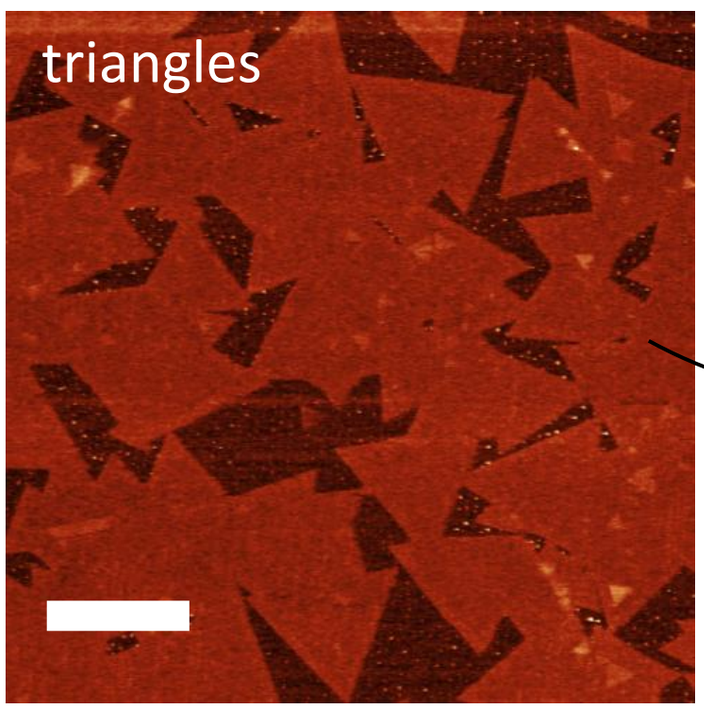
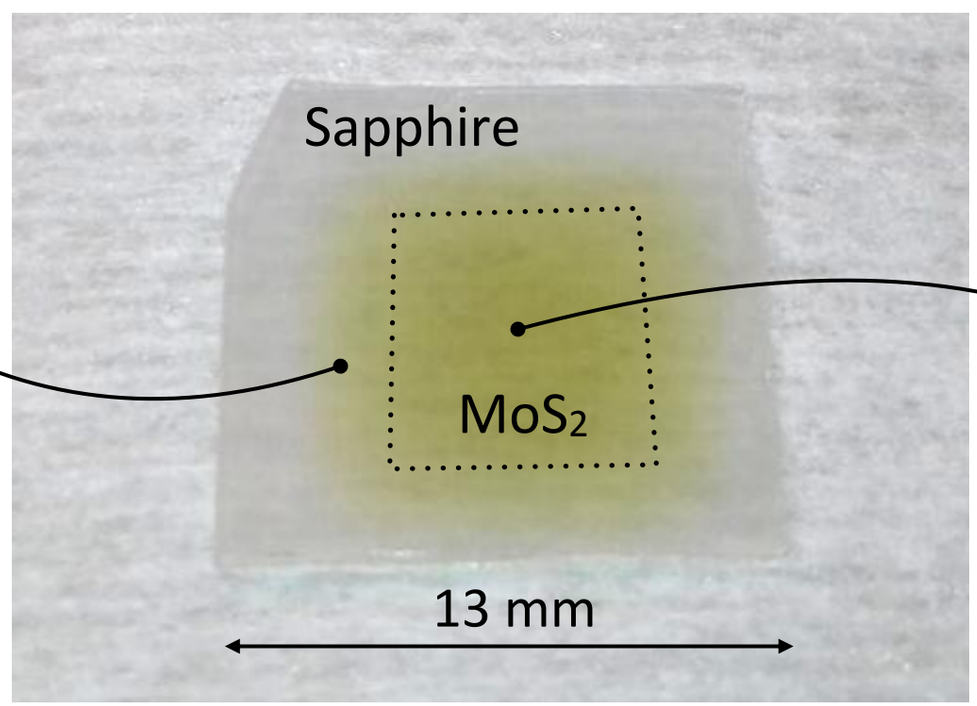
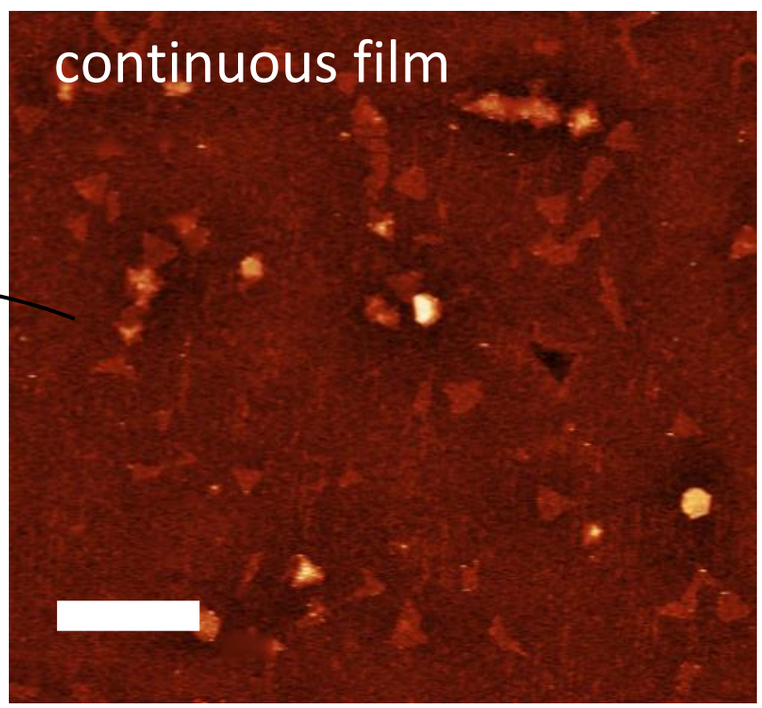
MoS_2 CVD-growth









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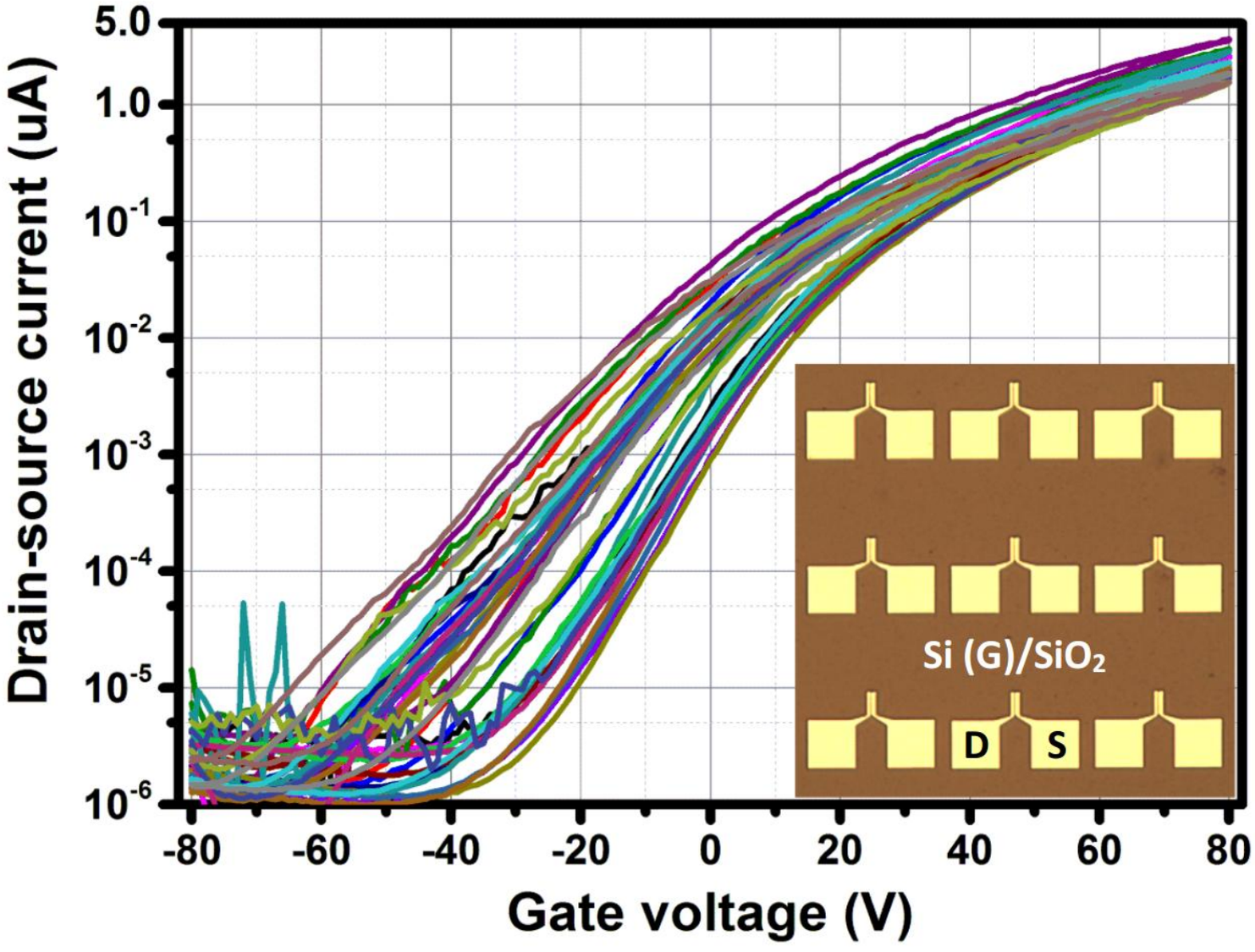
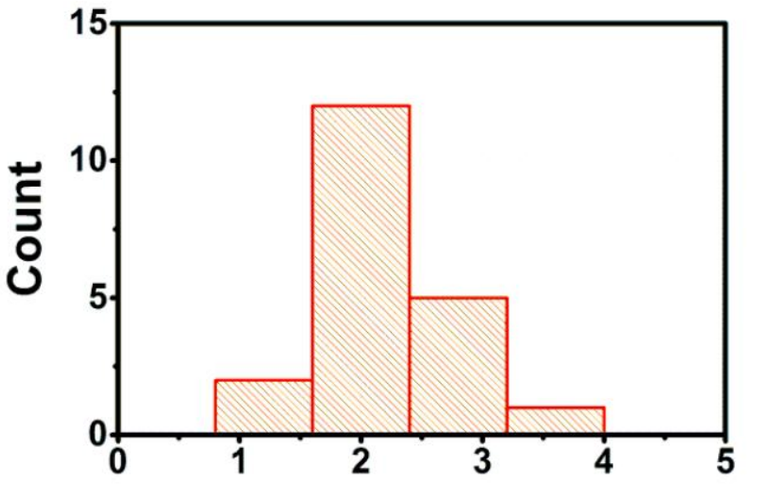
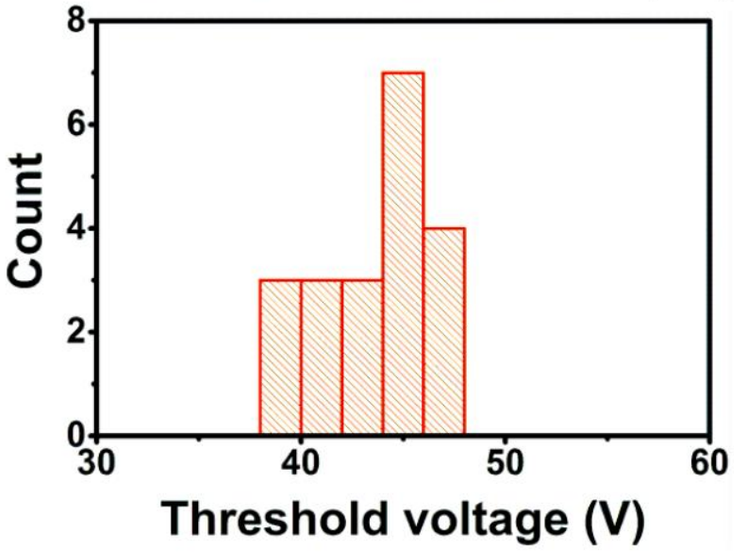
MoS_2 film uniformity







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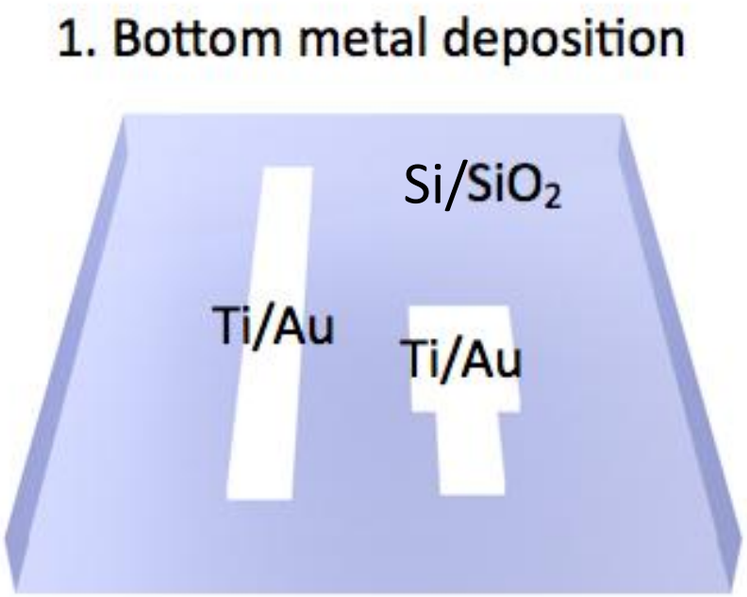
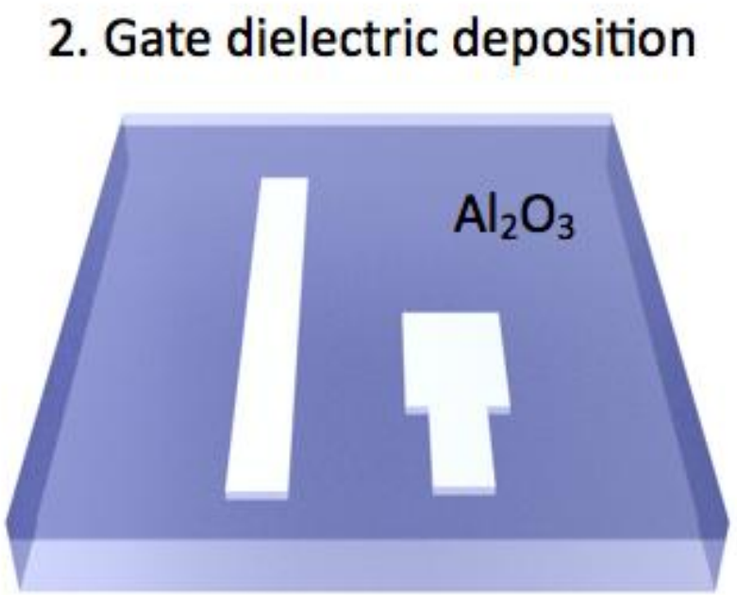
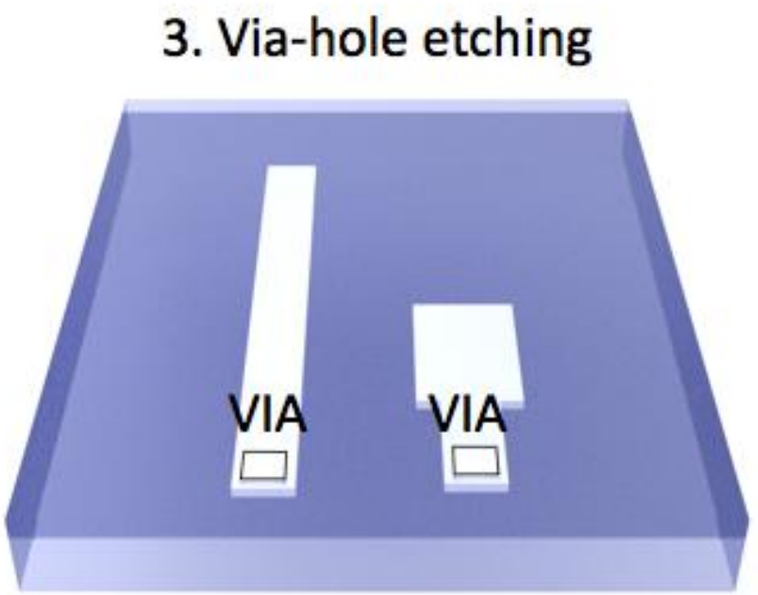
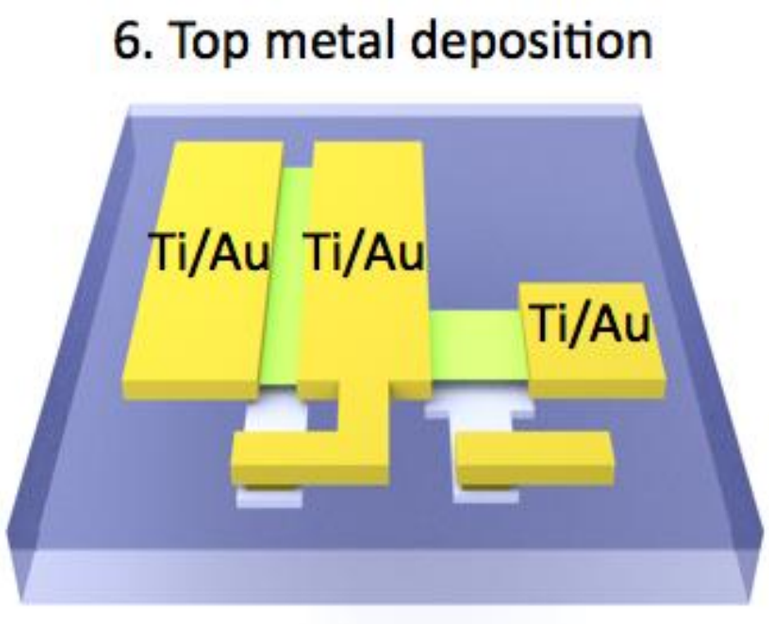
Gate-first technology









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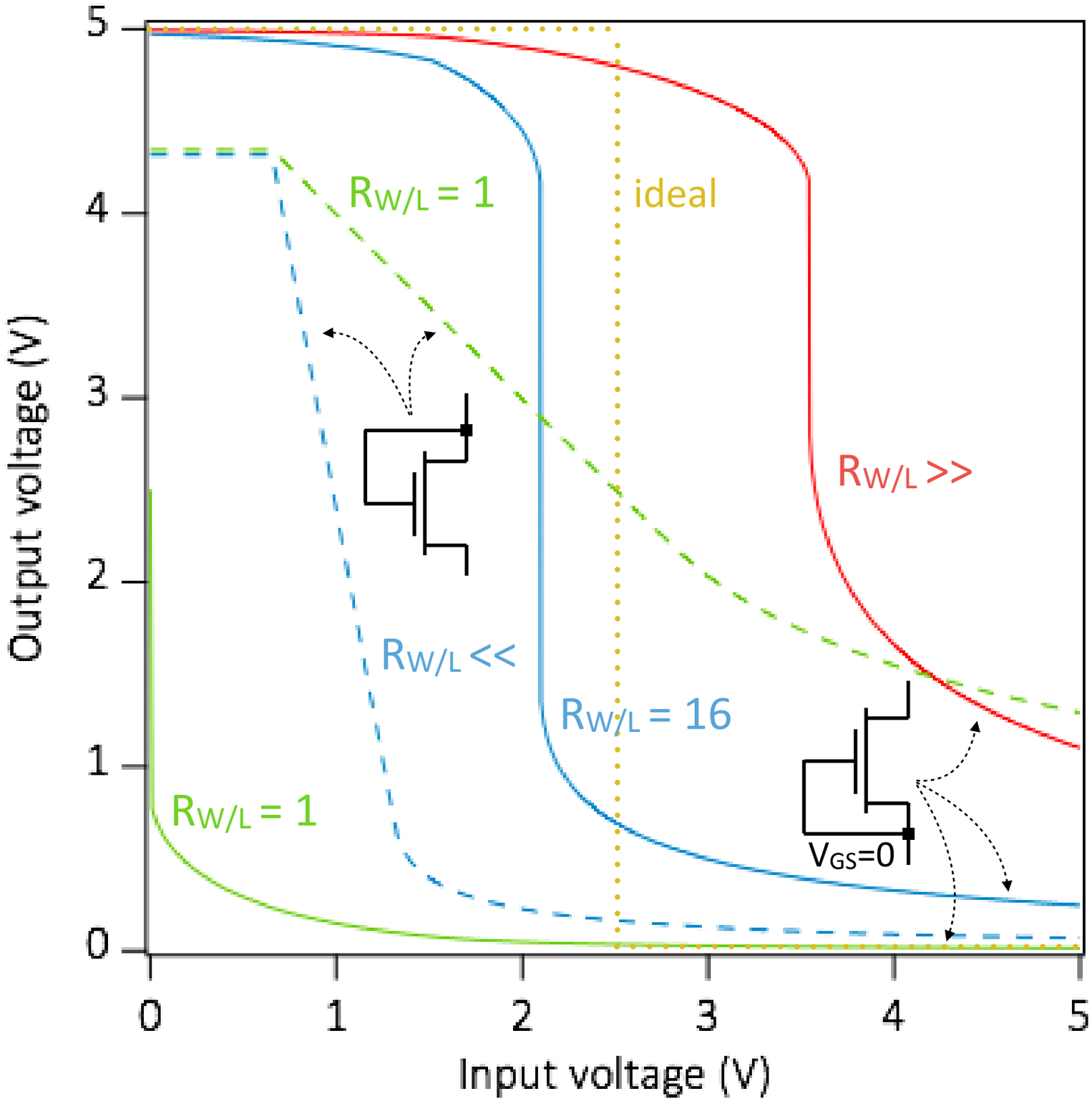
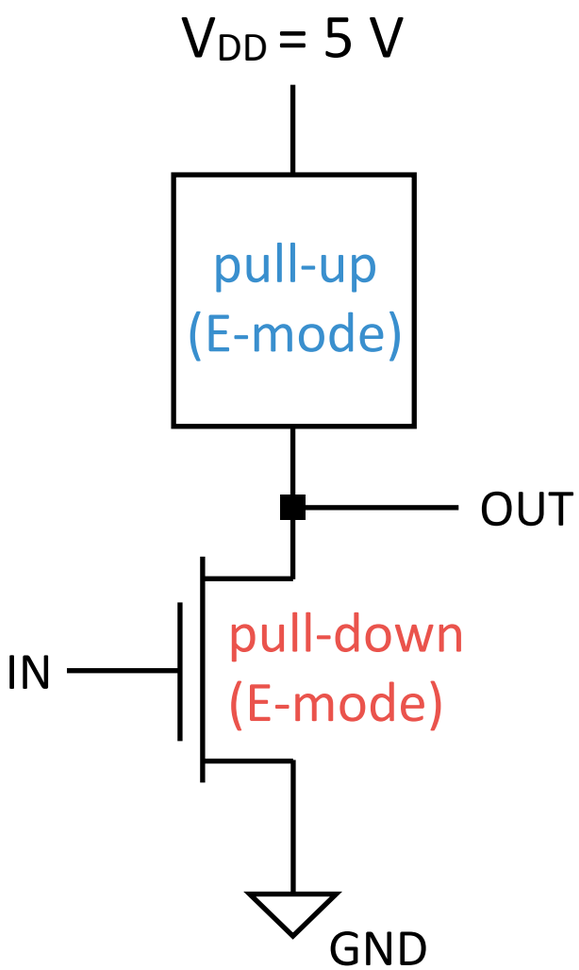
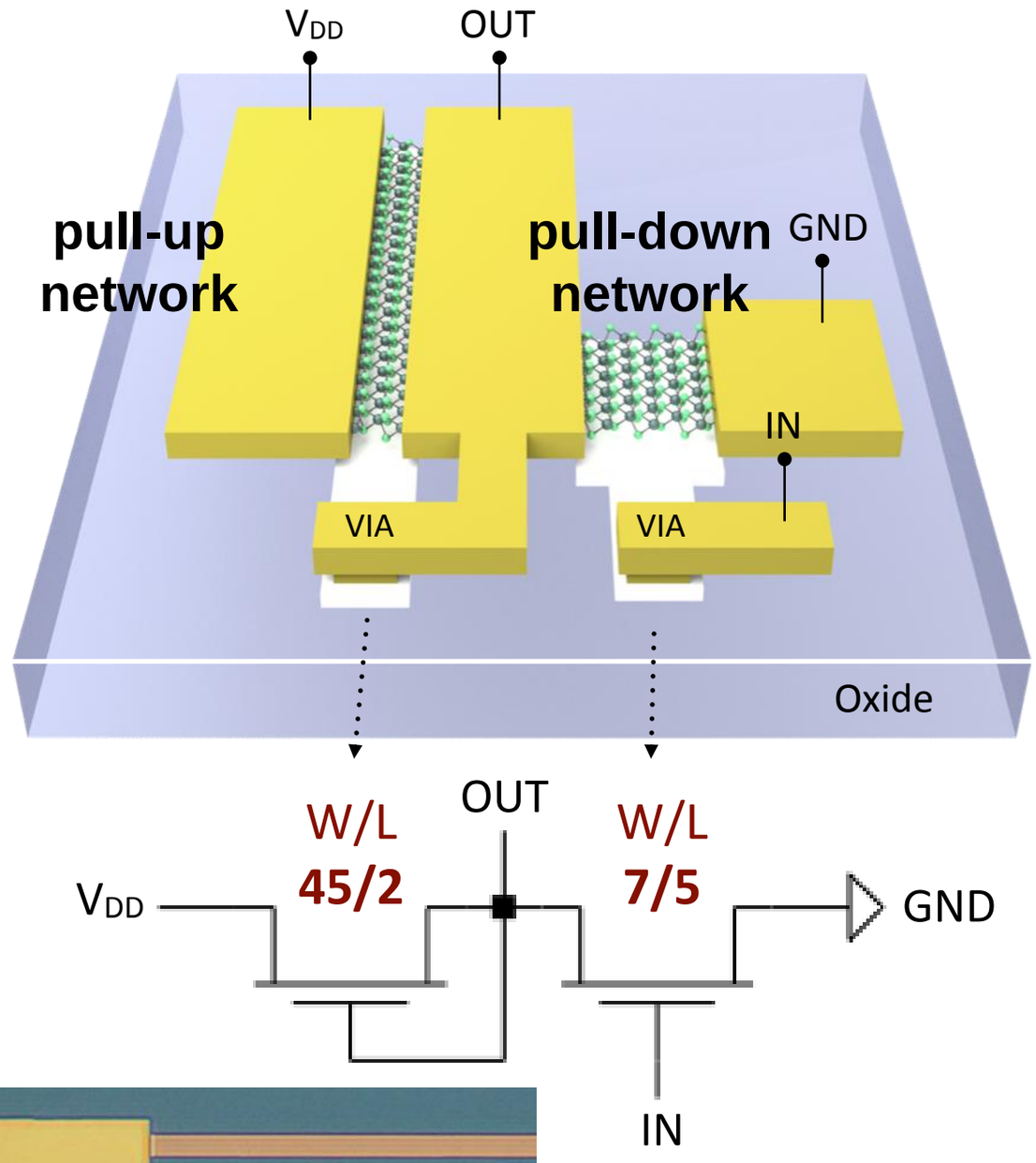
NMOS logic

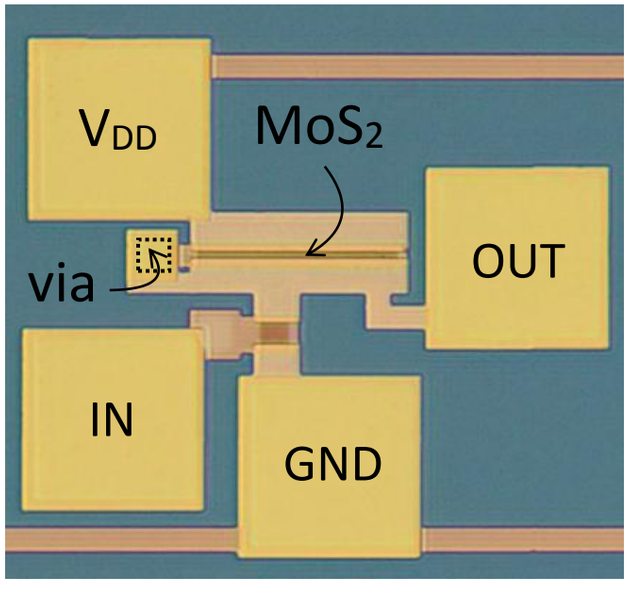


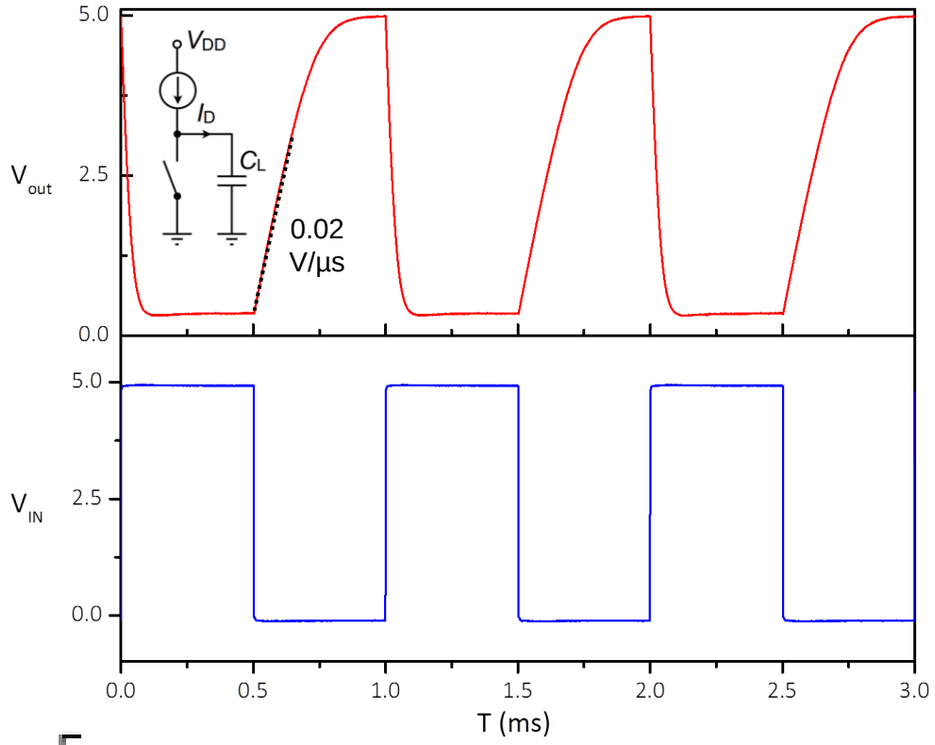


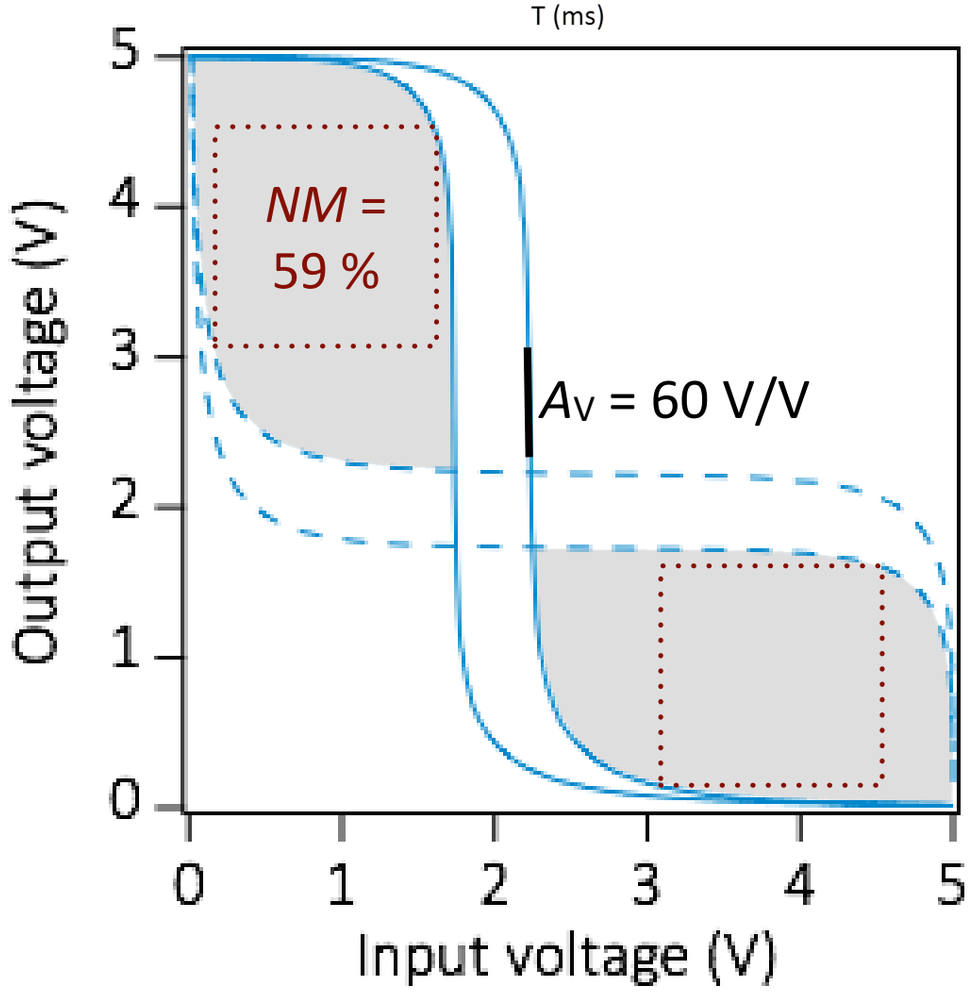
$$R_{W/L} = \frac{\left(\frac{W}{L}\right)_{\text{pull-up}}}{\left(\frac{W}{L}\right)_{\text{pull-down}}}$$

NMOS inverter









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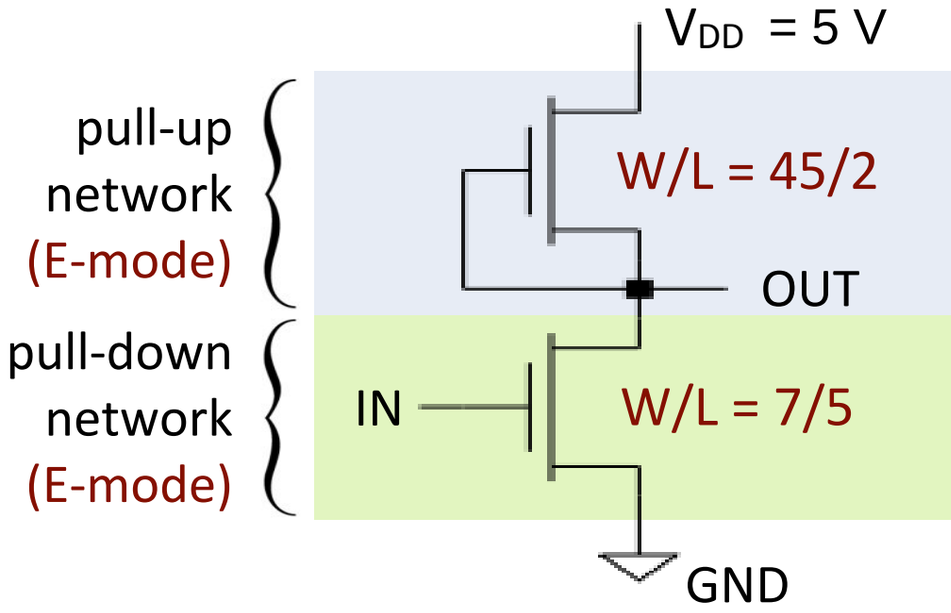
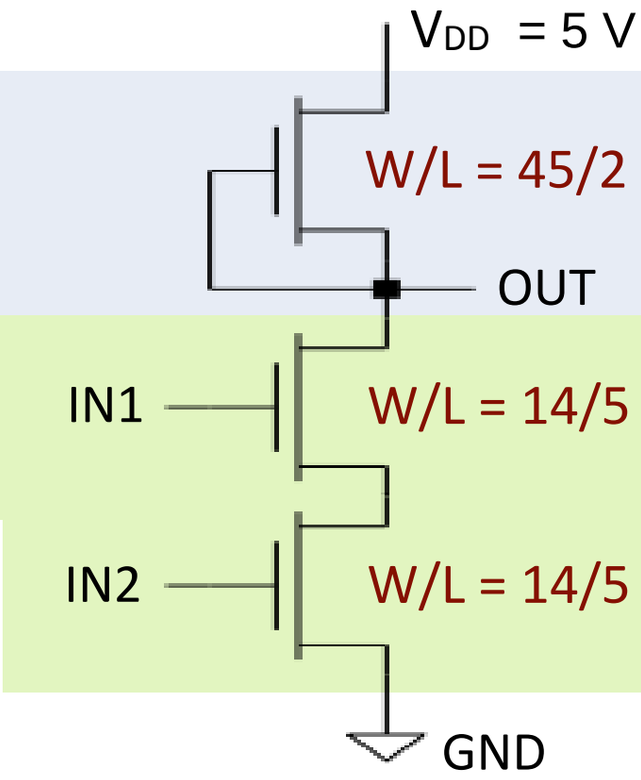
NMOS logic stages

INVERTER:



2-NAND:



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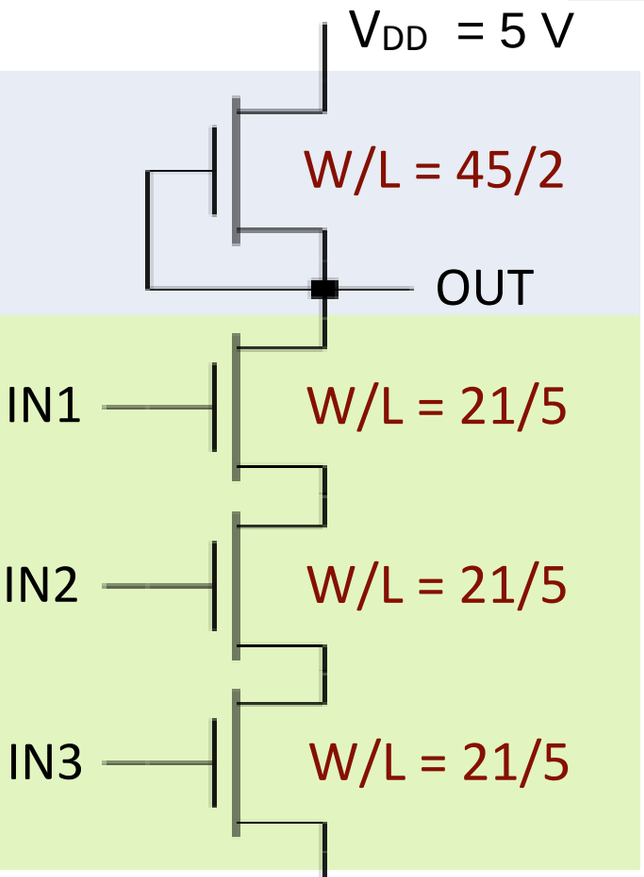

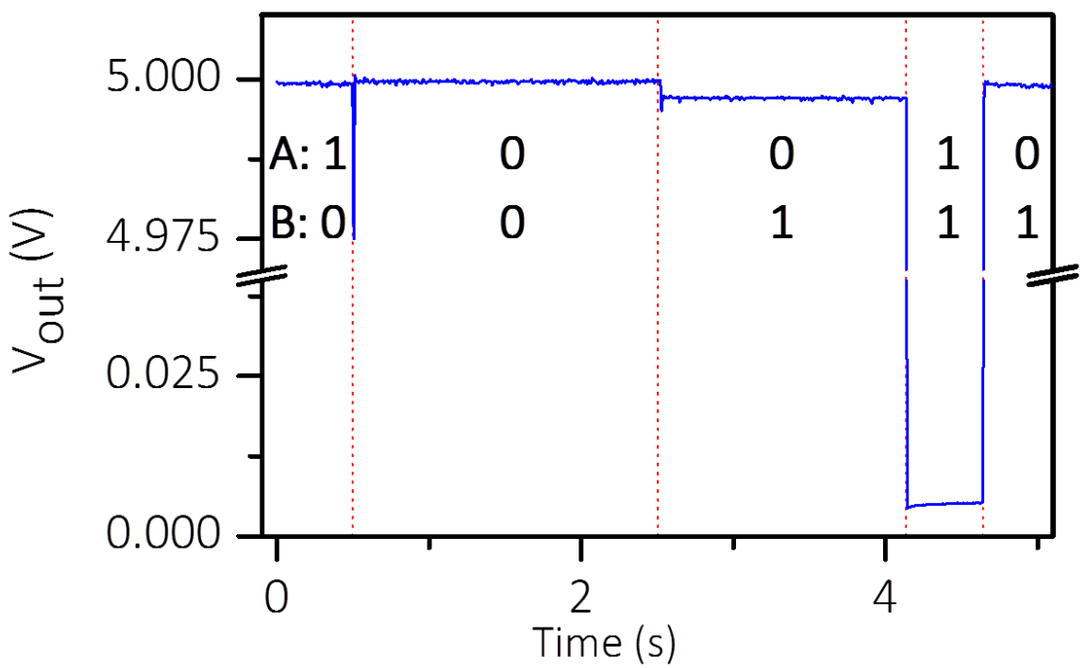

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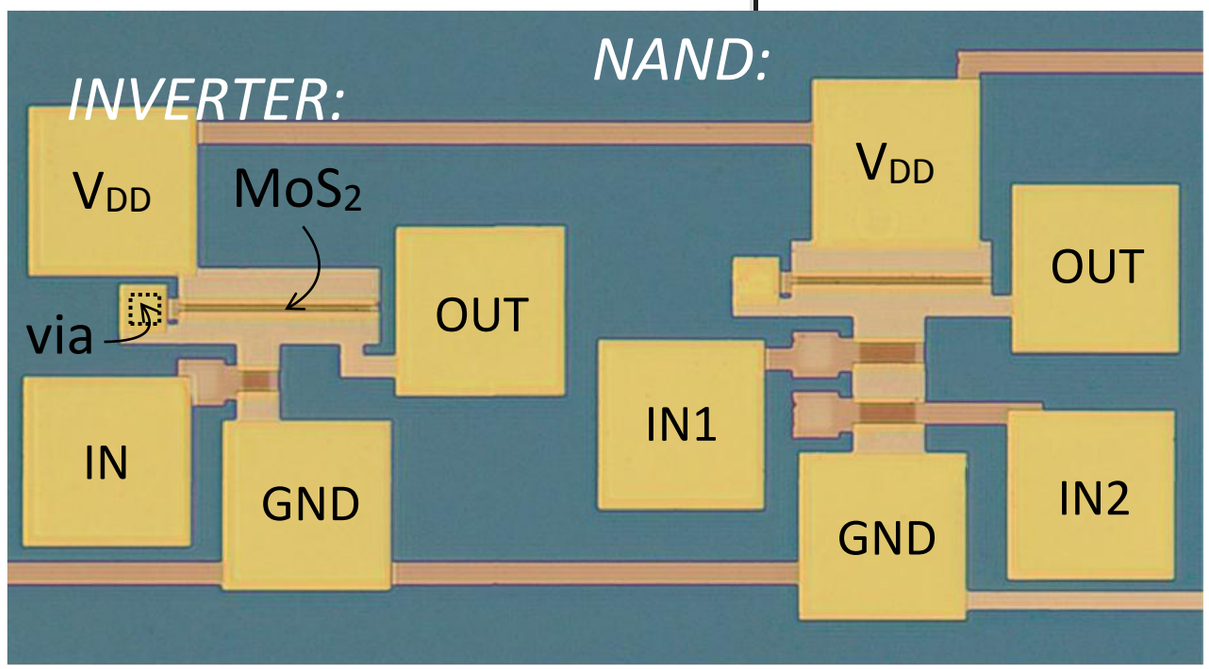

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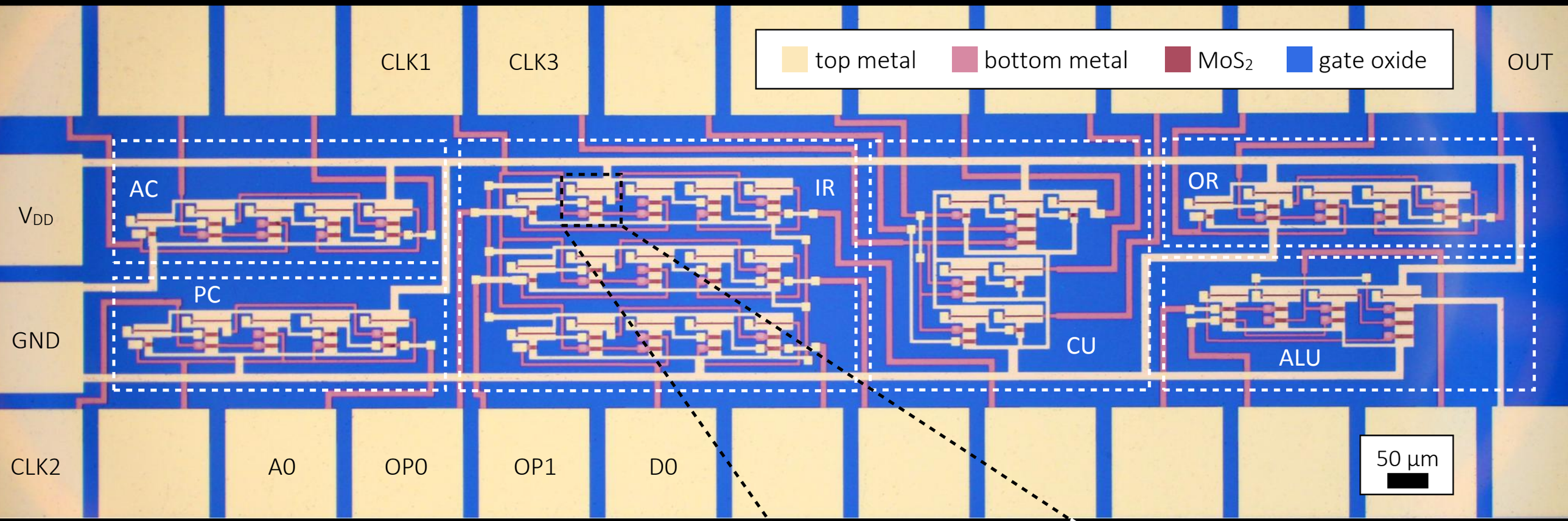
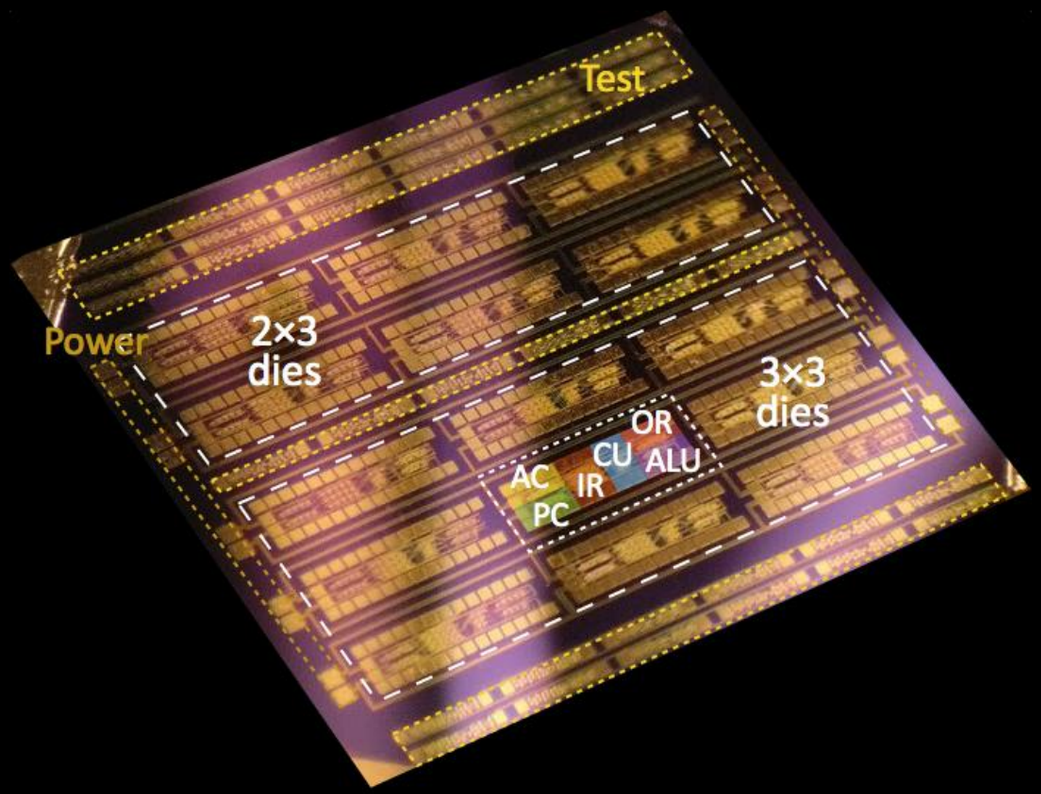
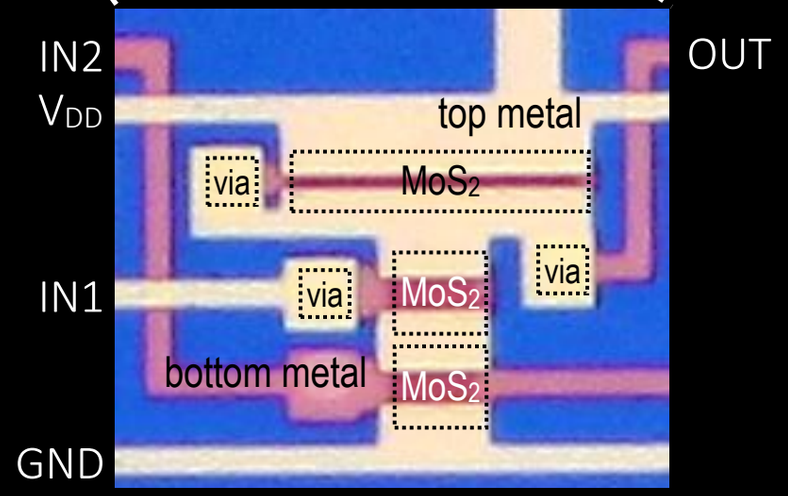
MoS_2 microprocessor







NAND-gate

115 transistors
A = 0.6 mm²
P_s = 60 µW

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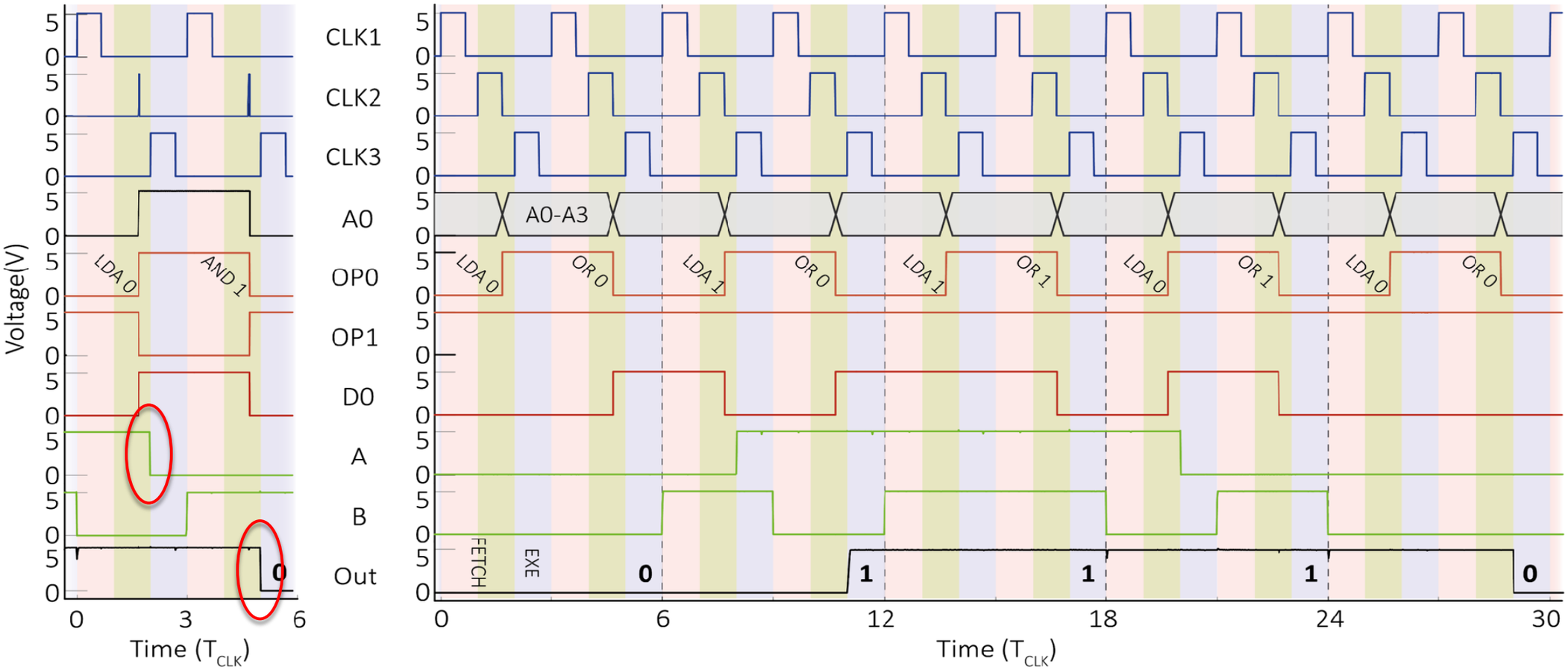
Device operation

Example 1:

LDA 0

AND 1

Example 2: series of logical disjunction operations



challenges:

- device uniformity
- contact resistance
- CMOS…

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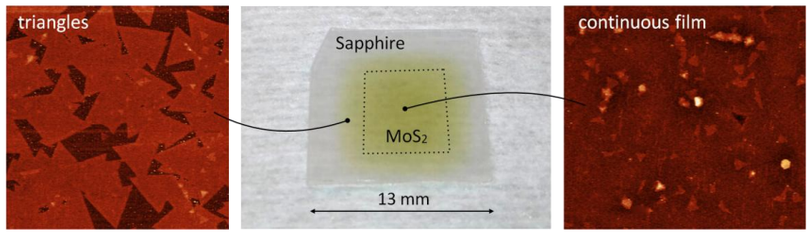
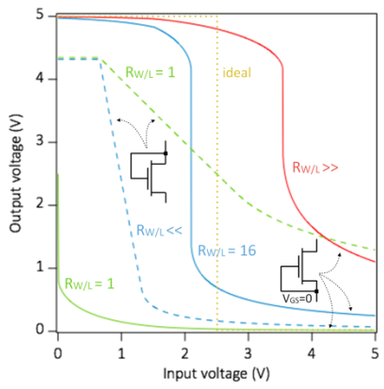
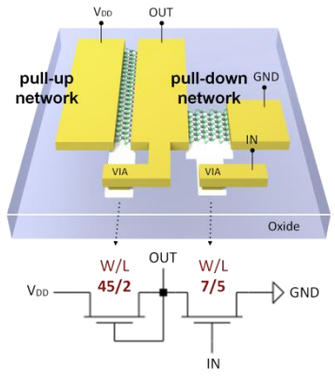
Summary

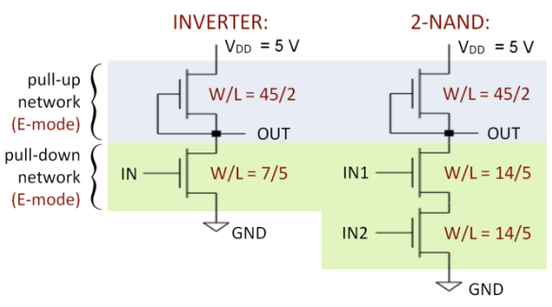
cm-scale uniform MoS_2 film growth



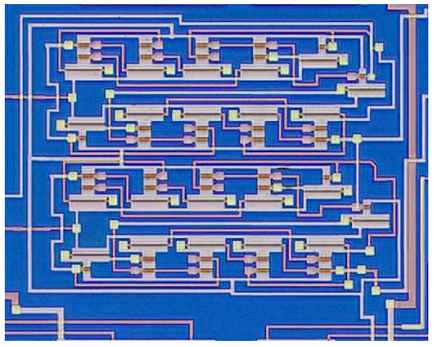
W/L ratio designed MoS_2 logic gates







→ Cascadable



large, complex circuits → microprocessor