Graphene 2017

March 28-31

Barcelona (Spain)

7th edition of the largest European Conference & Exhibition in Graphene and 2D Materials

Beyond silicon electronics-FETs with nanostructured graphene channels with high on-off ratio and high-mobility

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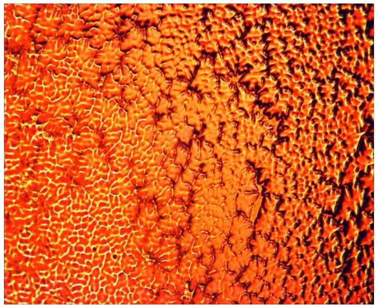
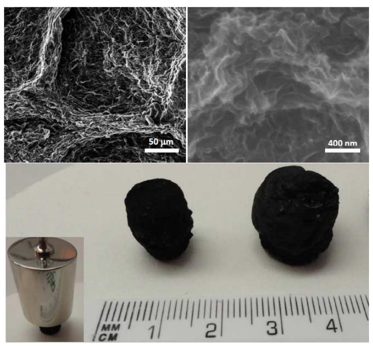
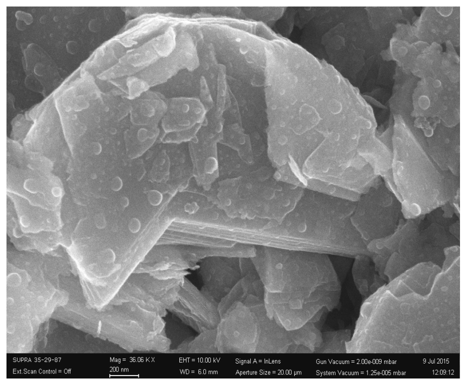
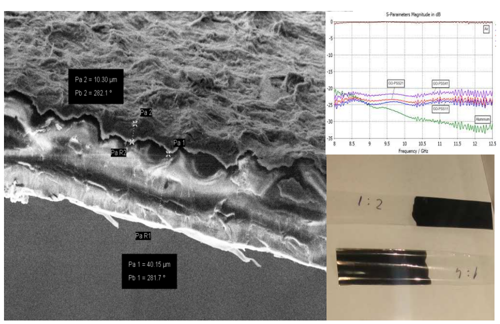
Research Centre for Integrated Systems Nanotechnologies and Carbon Based Nanomaterials- opened in dec.2015









Graphene oxide/PEDOT:PSS on PET de 40 µm;

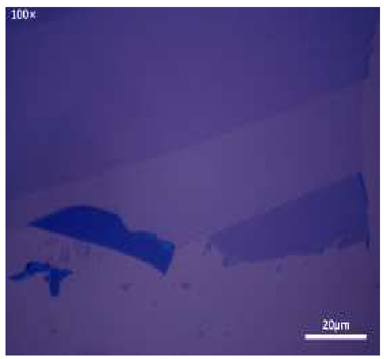
Equipments for : CVD for growing graphene; ALD; dielectric growth, MBE , metal deposition + Raman and FTIR spectroscopy in a 240 m^2 clean room with class 1000 , and some areas with class 100. 5 millions Euro investments (UE)

My life with graphene

Graphene ink- Nanointegris

2007

Graphene flakes



2007 from Manchester Univ. Prof. A. Geim and dr. Peter Blake

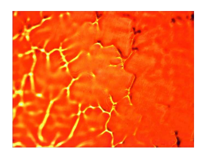
4 inch graphene wafer on HR Si – Graphene Supermarket

2012

4 inch graphene wafer on HR Si – Graphenea,Spaian

Towards 6 inch wafer

2014-2016

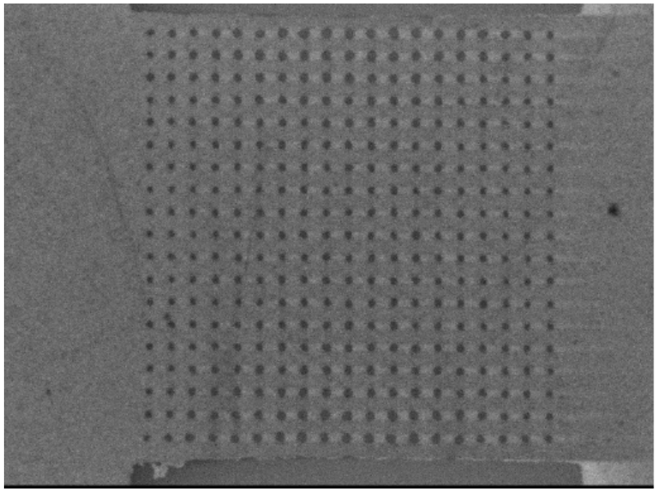


First CVD graphene grown in IMT Bucharest, january 2016

GRAPHENE ELECTRONICS CONUNDRUM :

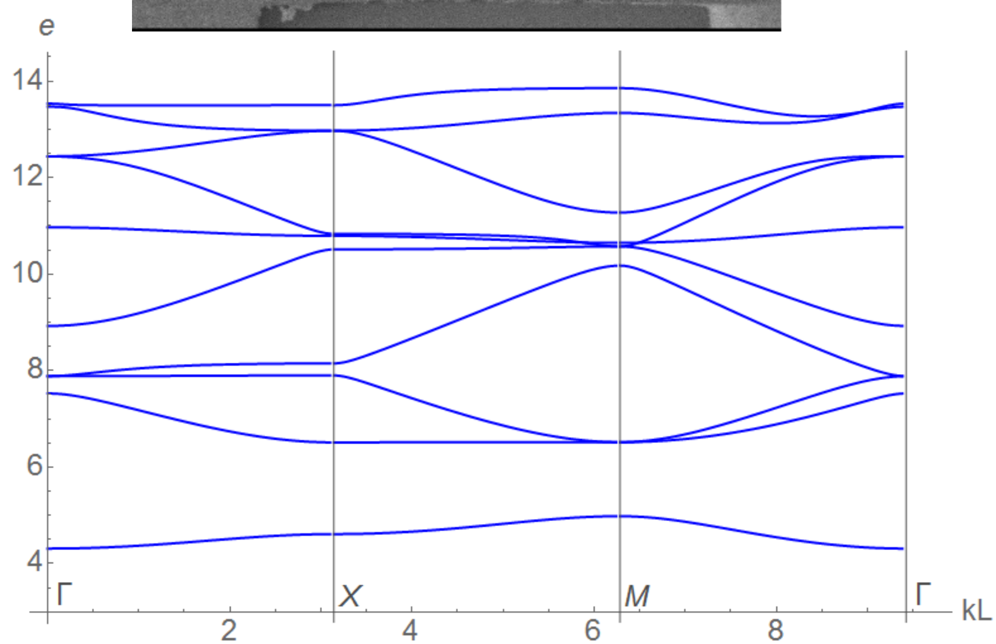
HIGH MOBILITY AND HIGH ON-OFF RATIO

- Graphene electronics was almost abandoned because the key electronic device – the graphene field-effect transistor (GFET), cannot be switched on and off due to the absence of a bandgap.
- How to solve the conundrum?
- GFET with a nanopatterned channel is a high-mobility, high on-off ratio FET.

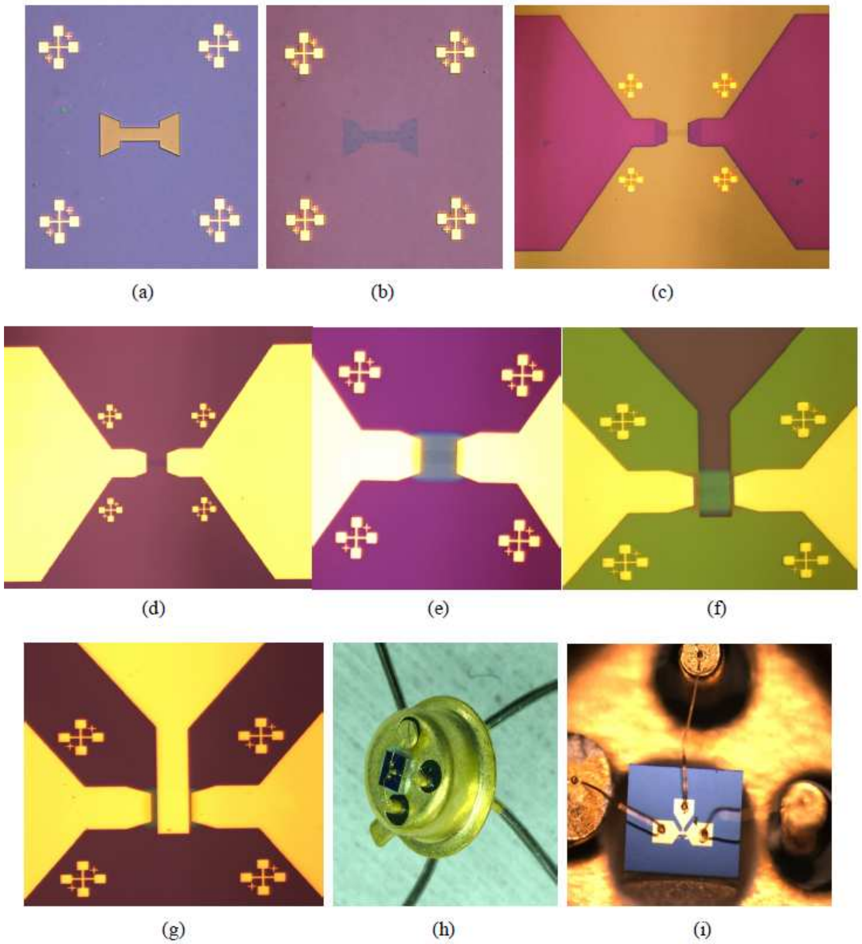


SEM image of a nanopatterned GFET channel with 2 μm.

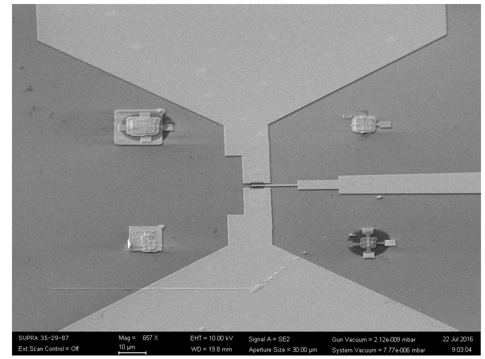
E_g=0.16 eV

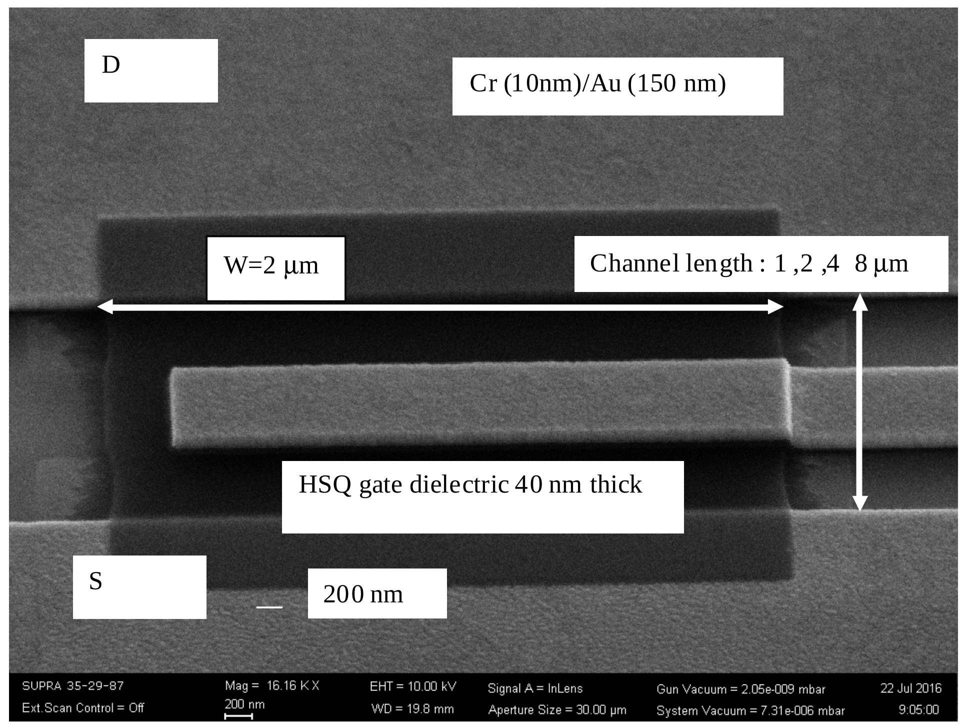


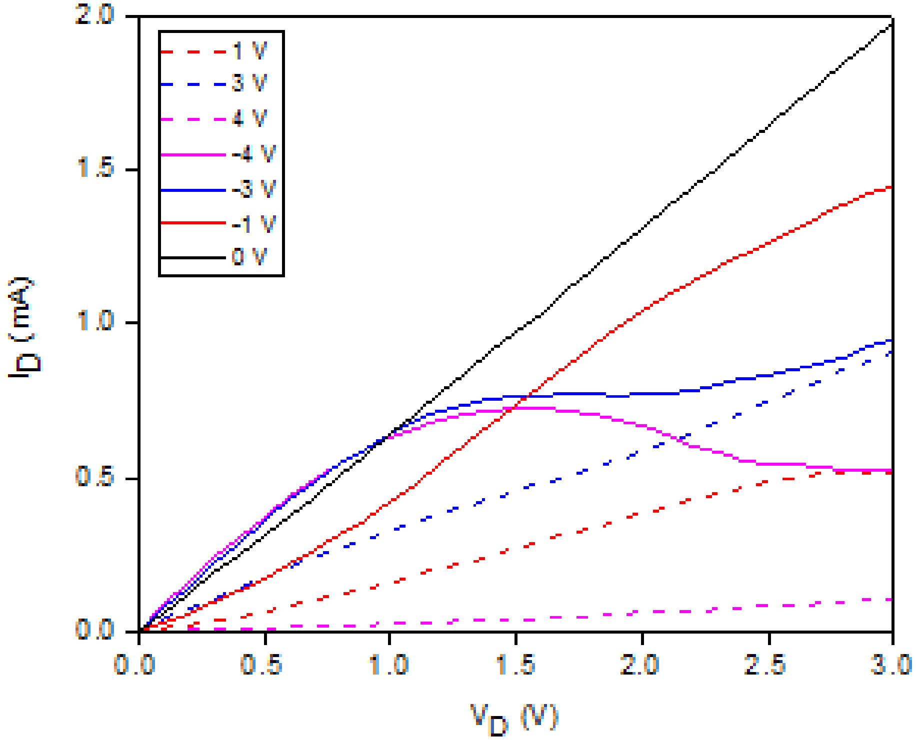
nanohole array with a period of 100 nm and a diameter of 20 nm the corresponding bandgap is about 0.16 eV, but this parameter increases to 0.2 eV if the nanohole diameter becomes 30 nm.

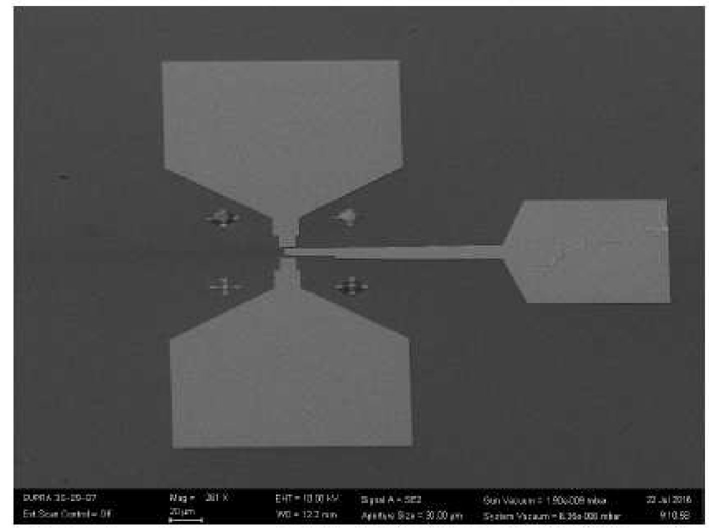


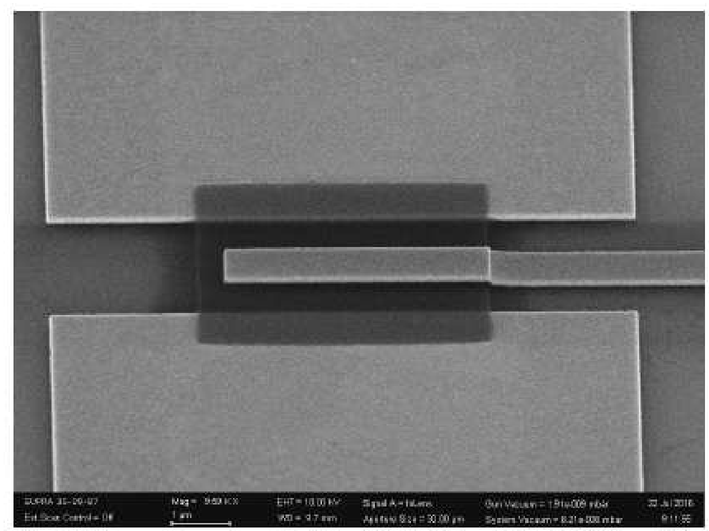
90 GFETs on a graphene chip cut from a 4 inch graphene wafer (CVD growth and transfer –Graphenea)-40 % are working very well







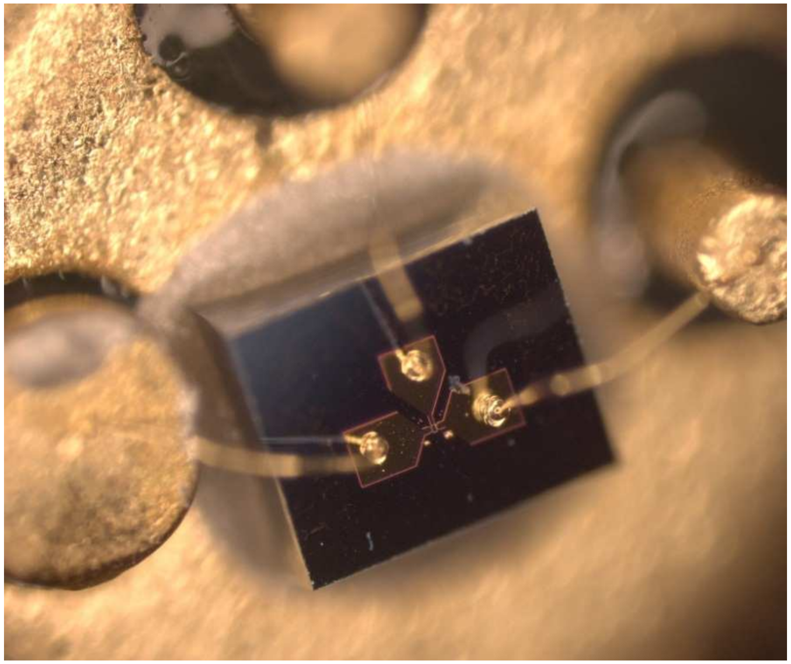

(a)


(b)

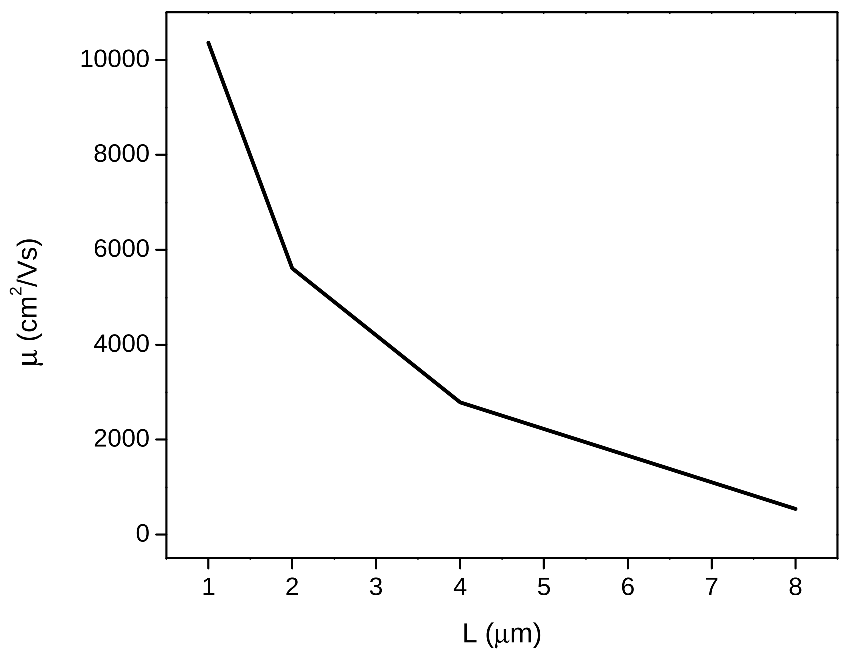
Drain current vs drain voltage characteristics of a nanoperforated GFET at various gate voltages indicated in the inset

- the drain current tends to saturate at some gate voltages, e.g. at 1 V and -1 V

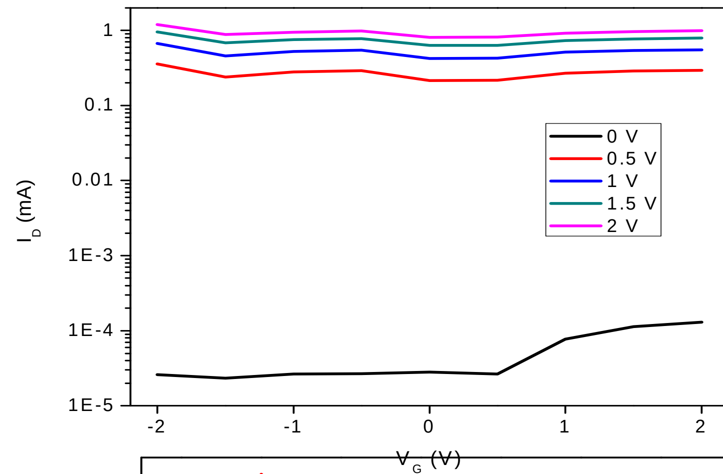
- a clear negative differential resistance region (NDR) appears at = -3 V and -4 V.



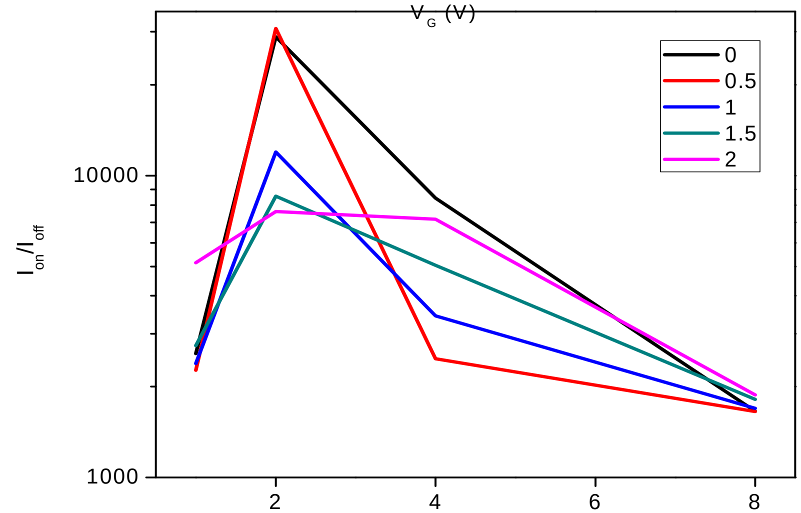
L = 2 μm



Mobility

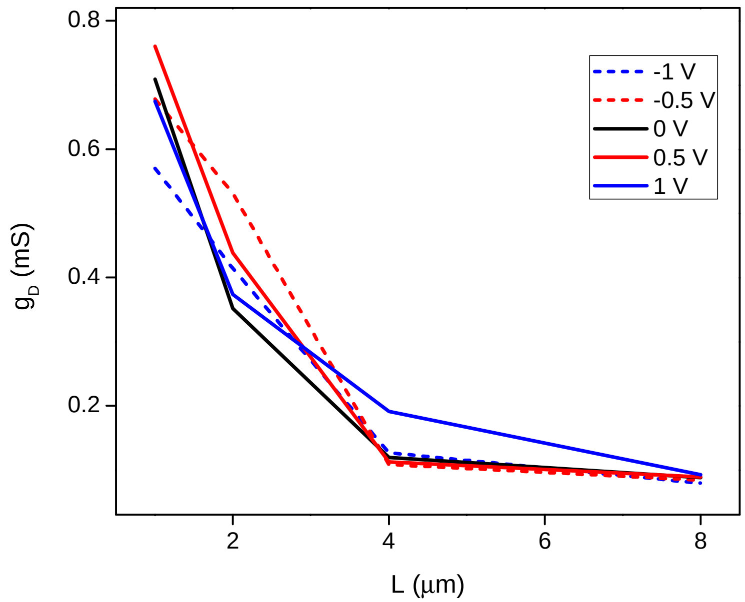


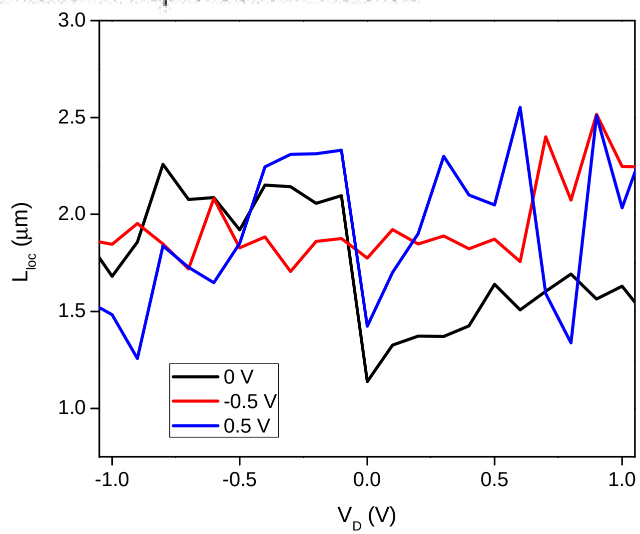
L=2 μm



the on/off ratio between drain currents at 0 V and 2 V as a function of the channel length for several gate voltages indicated in the inset.

on/off





$$g_D(L) = g_{d0}\exp(-L/L_{loc})$$

Strong localization L_{loc}=1.9µm

Long room temperature localization and phase coherence lengths (8 µm) could be explained by the nonuniform nanohole diameters in the transverse direction, which induces charge carrier focusing/guiding along the middle part of the channel such that the charge carriers avoid the boundaries of the channels and the associated strong recombination centers. These non-uniformities in the hole diameters are induced by the proximity effects due to e-beam lithography. For a nanohole array with a period of 100 nm and a diameter of 20 nm the corresponding bandgap is about 0.16 eV, but this parameter increases to 0.2 eV if the nanohole diameter becomes 30 nm. As a result, the charge carriers are guided through the central part of the channel and recombinations at channel boundaries are strongly reduced.

Thank you !

Romanian Research Centre for Carbon Based Nanomaterials – Electronics at atomic scale.