Tunneling field effect transistor based on $MoTe_2/MoS_2$ van der Waals heterojunction

Bondae Koo[1,2]
Gwang Hyuk Shin[1], Hamin Park[1], and Sung-Yool Choi[1,*]

[1]*School of Electrical Engineering, Graphene/2D Materials Research Center, KAIST, 291 Daehak-ro, Yuseong-gu, Daejeon, 34141, Korea*

[2]*System LSI, Samsung Electronics, 1 Samsung-ro, Giheung-gu, Yongin-Si, Gyeonggi-do, 17113, Korea*

sungyool.choi@kaist.ac.kr

Two-dimensional stacked semiconductors provide a superior material structure for band to band tunneling devices due to sharp band edge as well as their atomically flat thickness[1]. Among two-dimensional materials, $MoTe_2$ has a narrow band gap of 0.8 eV with small electron affinity and p-type characteristic[2]. In contrast, MoS_2 has a large electron affinity with a bandgap of 1.2 eV (ML) and n-type characteristic[3]. Therefore, a heterojunction of $MoTe_2$ and MoS_2 may have an appropriate band alignment in terms of band to band tunneling.

In this work, we demonstrate a tunneling field effect transistor based on the $MoTe_2/MoS_2$ van der Waals heterojunction. As a gate dielectric, 10nm-Al_2O_3 was deposited by ALD. Ti and Pd were used as S/D contact metal for MoS_2 and $MoTe_2$ respectively, which have appropriate work function in order to reduce contact resistances by lowering Schottky barrier heights[3,4].

Consequently, the $MoTe_2/MoS_2$ tunneling field effect transistor shows on/off current ratio of > 10^4. In the I_D-V_D curve, the tunneling currents were mesured at the reverse drain bias, while NDR-like behaviors were observed at the forward drain bias in room temperature. This phenomenon distinctly appeared as a function of the gate bias.

References

[1] Tania Roy et al., Applied Physics Letters, 8 (2016) 083111
[2] Nihar R. Pradhan et al., ACS Nano, 6 (2014) 5911-5920
[3] Wei Liu et al., 2013 IEEE International Electron Devices Meeting (2013) 19.4.1-19.4.4
[4] Saptarshi Das et al., Applied Physics Letters, 10 (2013) 103501

Figures

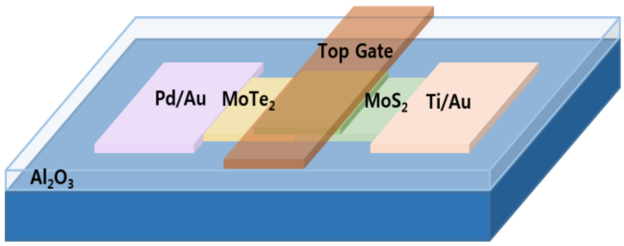

Figure 1: The illustration of a device structure

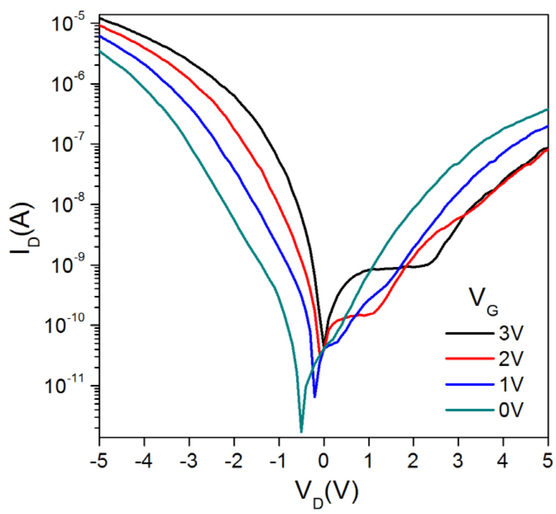

Figure 2: I_D-V_D electrical characteristics as a function of gate bias