Intrinsic rectification in gated CVD graphene ribbons

Pierre-Antoine Haddad.

Denis Flandre, Jean-Pierre Raskin

Université catholique de Louvain, Place du Levant 3, B-1348, Louvain-La-Neuve, Belgium

pierre-antoine.haddad@uclouvain.be

THz rectennas couple micron-size antennas and high-speed diodes to convert the incoming THz AC electric field to useable DC power. The non-linear electrical behavior required for rectification can be obtained from metal/insulator/metal (MIM) diodes [1]. These however present frequency limitations due to poor intrinsic RC response time and impedance matching. Geometric graphene diodes have been proposed to address these issues [2]. The ballistic transport of charge carriers in a funnel-shaped planar structure, with a funnel neck width smaller than the mean free path, has been discussed to induce a diode-like asymmetric electrical behavior. Electrical results on the I-V asymmetry $\Upsilon = |I_{DS}(+V_{DS})/I_{DS}(-V_{DS})|$ of these diodes have been reported with exfoliated graphene [2].

Here we investigate rectangular graphene ribbon FETs with the methodology described in [2] and report non-linear electrical characteristics without the particular funnelshaped channel. Commercially available CVD graphene is transferred on wafer-scale from its Cu catalyst to a thermally grown 20 nm-thick silicon dioxide layer on a lightlydoped silicon substrate with an aluminum back-gate (Fig. 1). The 3 µm long and 30 µm wide graphene channels are defined and contacted using optical lithography. Kelvin probe DC measurements are performed at room temperature and at 77 K under vacuum conditions and exhibit a gatecontrolled diode-like asymmetric behavior between forward and reverse biases of the

same amplitude as reported by [2] (Fig. 2) at both temperatures.

The results are explained by SPICE simulations and related to the slight change in graphene conductivity due to the V_{DG} voltage variations. This may be of interest for graphene interconnect considerations as well as circuit designs using graphene FETs.

References

- [1] K. Choi et al., IEEE Transactions on Electron Devices, vol. 58 no. 10 (2011) pp. 3519–3528.
- [2] G. Moddel et al., Solid State Communications, vol. 152 no. 19 (2012) pp. 1842–1845.

Figures

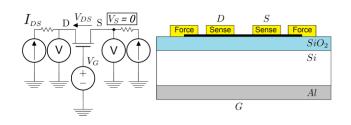


Figure 1: Measurement setup schematic (left) and 4-contact fabricated structure (right).

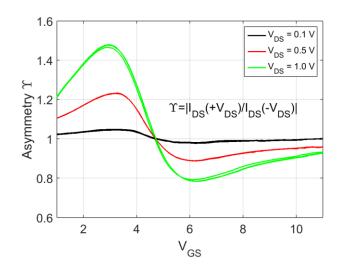


Figure 2: Three asymmetry curves measured at 77 K are shown per V_{DS} for the same device.