Statistical study of passivation effects on graphene field effect transistors (GFETs) for RF/Optoelectronic applications

Odile Bezenecenet[1]
Sana Mzali[1], Alberto Montanaro[1], Marie-Blandine Martin[1], Pierre Legagneux[1], Raphaël Aubry[1], Bruno Dlubak[2], Pierre Seneor[2], A. Centeno[3], A. Zurutuza[3], Stephan Hofman[4], John Robertson[4]

1. Thales Research and Technology, 91767 Palaiseau, France
2. Unité Mixte de Physique CNRS/Thales, 91767 Palaiseau, France, and University of Paris-Sud, 91405 Orsay, France
3. Graphenea S.A. A75022608 Tolosa Hiribidea 76 20018 Donostia-San Sebastián, Spain
4. Department of Engineering, University of Cambridge, Cambridge CB21PZ, United Kingdom
Odile.bezencenet@thalesgroup.com

Graphene has gained increasing attention over the last decade, due to its outstanding properties closely linked to its 2D material nature[1]. In particular, the potential of graphene for optoelectronic applications is currently being extensively explored because of its ultra-high carrier mobility and absorption from the far infrared to the ultraviolet [2,3]. However, to construct high-quality RF/optoelectronic devices, it is necessary to control accurately graphene doping and to operate highly stable devices.
Here, we report on statistical analysis and consistency of electrical performances of devices based on a large scale passivated graphene platform [4]. More than 500 graphene field effect transistors (GFETs) were fabricated and tested. We characterized the potential of a two-step encapsulation process including an Al_2O_3 passivation layer to avoid graphene contamination during the fabrication process (called protection layer) followed by a final Al_2O_3 passivation layer at the end of the GFET fabrication.

The impact of each layer on our GFETs performance has been statistically demonstrated by comparing 3 different fabrication processes (Fig. 1). While we do not observe any conductance minimum with unprotected and unpassivated devices, 75% of the protected/passivated GFETs and 58% of only protected devices exhibit a conductance minimum for a gate voltage (V_G) below 50 V. Successful hysteresis free DC characteristics were achieved on about one-quarter of the protected/passivated GFETs.

These results highlight the importance of the use of both protection and passivation layers to fabricate low-doped graphene devices with minimum hysteresis.

This work was funded through the European projects Grafol and Graphene Flagship

References

[1] Novoselov K. S., et al., Nature, 7419 (2012) 192.
[2] Bonaccorso F., et al., Nature Photonics, 9 (2010) 611
[3] Geim A.K. & Noveselov K.S., Nature Materials, 3 (2007) 183
[4] S. Mzali, et al., Appl. Phys. Lett. 109, 253110 (2016)

Figures

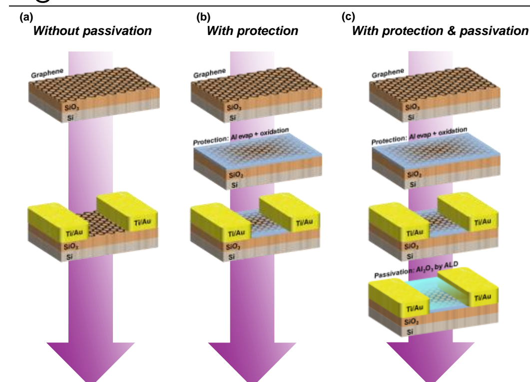

Figure 1: Process Flows of graphene devices fabrication