Existence of nontrivial topologically protected states at grain boundaries in bilayer graphene: signatures and electrical switching

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Recent experiments [1] confirm the existence of gapless states at domain walls created in gated bilayer graphene, when the sublattice stacking is changed from AB to BA. These states are significant because they are topologically protected, valley-polarized and give rise to conductance along the domain wall. Current theoretical models predict the appearance of such states only at domain walls, which preserve the sublattice order. Here we show that the appearance of the topologically protected states in stacking domain walls can be much more common in bilayer graphene, since they can also emerge in unexpected geometries, e.g., at grain boundaries with atomic-scale topological defects. We focus on a bilayer system in which one of the layers contains a line of octagon–double pentagon defects that mix graphene sublattices. We demonstrate that gap states are preserved even with pentagonal defects. Remarkably, unlike previous predictions, the number of gap states changes by inverting the gate polarization, yielding an asymmetric conductance along the grain boundary under gate reversal. This effect, linked to defect states, should be detectable in transport measurements and could be exploited in electrical switches. [2]

References

[1] L. Ju, et al., Nature, 2015, 520.
[2] W. Jaskólski, M. Pelc, Leonor Chico and A. Ayuela. Nanoscale, 2016,8, 6079.

Figures

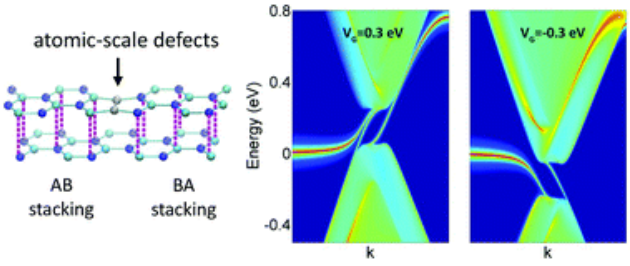

Figure 1: (Left) Detailed view of the AB–BA stacking. Different sublattices are boundary coloured in blue and cyan. The nodes which mix the two sublattices are depicted in grey colour. LDOS(E,k) calculated in the defect line region of BLG. Gate voltage applied to the undefected layer is V = 0.3 eV (Middle) and V = −0.3 eV (Right). The wavevector k corresponds to the direction along the defect line in reciprocal units where a is the unit cell width.