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In-situ Electrical Characterization of Atomic Layer Deposition of Top Gate Dielectrics for 2D TMD Transistors

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Abstract
Atomic layer deposition (ALD) is one of the most practical thin film deposition techniques for gate dielectrics for advanced CMOS technology since year 2007 when Hf based gate dielectrics were introduced. When ALD is applied to deposit on top of 2D materials, it is commonly reported that a surface treatment is introduced to modify surface characteristics and then followed by top gate dielectric deposition or passivation layer formation using ALD. Those surface treatment and ALD process directly impacts on backgated 2D field-effect-transistor (FET)'s transfer characteristics as shown in Fig. 1. Although it is critical to understand the effects of processes on 2D FETs performance, there are not many reports on effects of individual process steps, such as surface treatment, a half-cycle of ALD, particularly initial cycles.
In this presentation, I will introduce a new UHV clustered system connected both ALD and plasma treatment chamber to a probe station under vacuum for in-situ electrical measurement as shown in below figure. I will also discuss effects of nitrogen radical treatment and consecutive ALD process with tri-methyl Al and ozone on MoS_2 backgated FET's transfer characteristics.

Figures

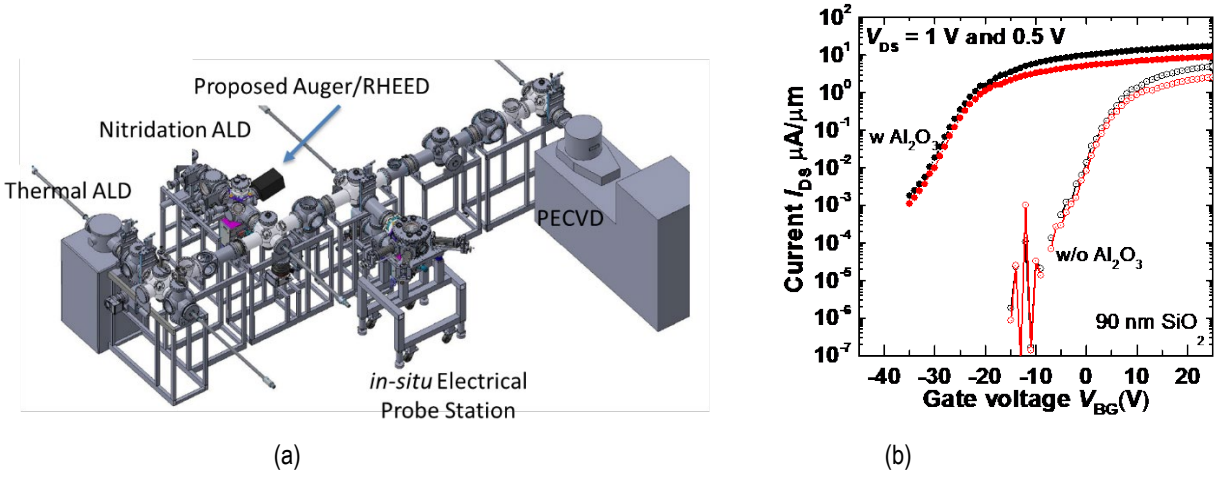

Figure 1: (a) Schematics of in-situ electrical characterization system clustered with thermal ALD and plasma treatment chambers (b) back-gate transfer characteristics of MoS_2 transistors with and without ALD Al_2O_3