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Field emission from WSe_2: A vertical field effect transistor

Francesca Urban, Niall McEvoy, and Antonio Di Bartolomeo
Institut de Science et d'Ingénierie Supramoléculaires, 8 Allée Gaspard Monge, Strasbourg, France
francesca.urban@unistra.fr

Electric control of carrier concentration by gate biasing, in field-effect transistor structures, is an effective way to tune the doping level of semiconducting materials. Such strategy is viable, for instance, in field emission (FE) applications, where electrons are extracted from the material by quantum tunnelling through the surface potential barrier upon the application of a strong electric field. FE is of great relevance to a variety of applications, ranging from electron microscopy and lithography to display technology or vacuum electronics. Indeed, lateral field emission transistors have recently gained popularity due to their potential for many high-frequency and high-power applications [1-2].

The gate control of doping and therefore of the FE current is particularly effective when the cathode is made of a low-dimensional material [3]. We report the first observation of gate-controlled field emission current from a tungsten diselenide (WSe_2) monolayer, synthesized by chemical-vapour deposition on SiO_2/Si substrate. Ni contacted WSe_2 monolayer back-gated transistors, under high vacuum, exhibit n-type conduction, suitable for field emission.

The electron emission, at 400 nm distance between anode and cathode, occurs under an electric field ~100 V/µm and exhibit good time stability. Remarkably, the field emission current can be modulated by the back-gate voltage. The first field-emission vertical transistor based on WSe_2 monolayer is thus demonstrated and can pave the way to further optimize new WSe_2 based devices for use in vacuum electronics [4].

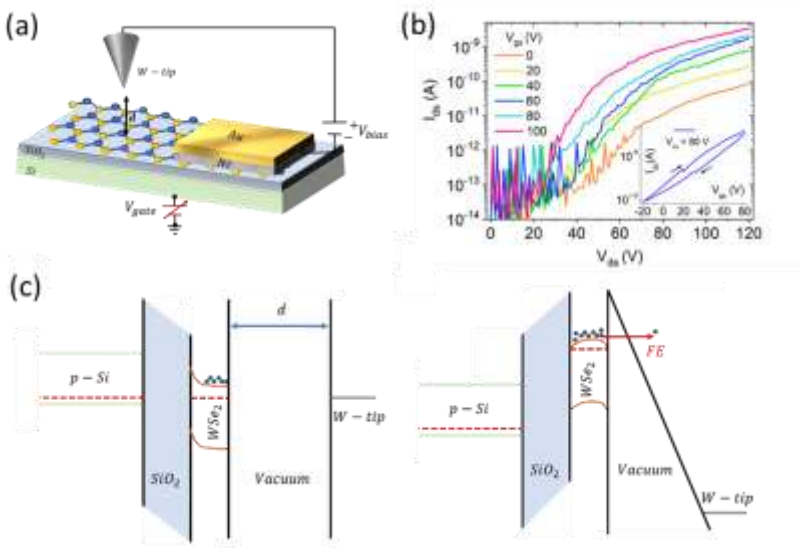

Figure 1: (a) Layout of a back-gate FE transistor with a WSe_2 monolayer channel over a SiO_2/Si substrate. (b) FE current measured at given back-gate voltages (V_{ds} steps of 1 V). (c) Band diagram for the unbiased device (left panel) and for the device under $V_{ds} > V_{gs} > 0$ V bias condition (right panel).

References

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